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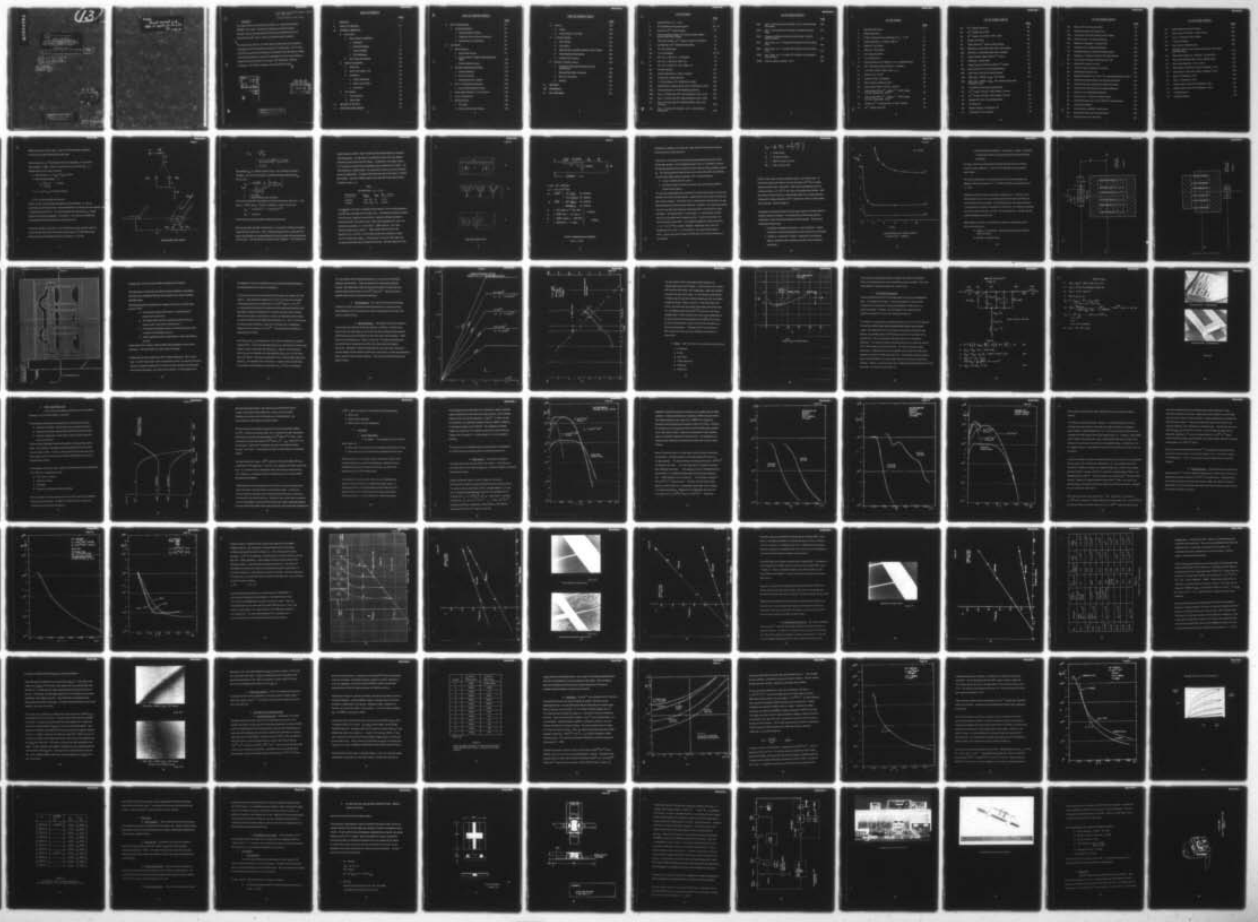

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I. ABSTRACT

This report describes work performed at Avantek, Inc. under Contract Number N00014-75-C-1163. Funding for the program was provided by Naval Electronic Systems Command and Naval Air Systems Command with technical administration by Mr. Eliot D. Cohen of the Naval Research Laboratory.

This report covers work on a 12 month (Phase I) program which had the objective of developing a FET and amplifiers covering the 7-15 GHz range. A 0.5 micron gate FET was successfully developed and the amplifiers were delivered on schedule. Technology development to improve FET performance as well as new techniques in amplifier design are discussed in this report. FET performance, materials development, and amplifier components are also described in detail.

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III. TECHNICAL NARRATIVE

A. Device Work

1. Device Design and Performance

a. Introduction: In the proposal which led to the present contract, the design of a suitable FET was discussed in some detail. The discussion ultimately led to a proposed design layout for an FET which would have a noise figure of less than 5 dB at 18 GHz, and a gain of approximately 10 dB. In this section, the design of the FET will be reviewed and the results obtained with geometries used in the program will be described. Test results and measured parameters will be compared to those predicted from the model and to the RF performance.

b. Horizontal Geometry: The initial decision to be made in the design of an FET is that of the gate dimensions. Gate length determines:

- C_{gs}, the gate to source (input) capacitance
- τ_g, the transit time for carriers under the gate

For the type of FET under consideration here, the carriers (electrons) are moving at the saturated velocity for electrons in gallium arsenide, about 1.5×10^7 cm/sec. Therefore, for a 0.5 micron gate:

$$t = \frac{d}{v}$$

$$= \frac{0.5 \times 10^{-4}}{1.5 \times 10^{7}}$$

$$\simeq 3.33 \text{ ps}$$

At 18 GHz, $\tau = 1/\omega = 55$ ps, and the transit time under the gate represents a phase delay of about 21°. Adequate performance can be obtained with this amount of shift.

A gate length of 0.5 micron represents an achievable state of the art value for present photolithographic technology. At the start of this program, it was known that 0.5 micron gate lengths could be manufactured with yields adequate to support the program itself. Indeed, in the course of a year, a process has been developed which yields 1/2 micron gates with good uniformity. Therefore, the decision to use 0.5 micron gate length was based on two considerations:

- It would achieve the performance required
- The processing required gave reasonable yields

Next the gate width (i.e. the larger dimension) must be determined. Gate width will affect:

a. g_m, transconductance
b. C_{gs}, gate to source capacitance
c. $f_T \cong g_m/2\pi C_{gs}$
d. Z_{in}, Y_{11}, S_{11}, etc.
e. Power output

In (c) above, both g_m and C_{gs} are proportional to W_g, the gate width. Thus, f_t should be independent of gate width. However, as a device is usually made larger by iteration, C_{gs} will include a parasitic component which will tend to reduce f_T.

With the exception of d and e above, almost all of the performance parameters of the FET are second order functions of gate width.

Since the gate area (L_g X W_g) determines the input capacitance, it also sets the input impedance. Figure 1 shows an equivalent circuit of the FET gate. It is desirable from a circuit point of view that:

1. Input Q be low, i.e., X_{Lgb} and X_{cgs} be small
2. Input be below resonance, i.e.

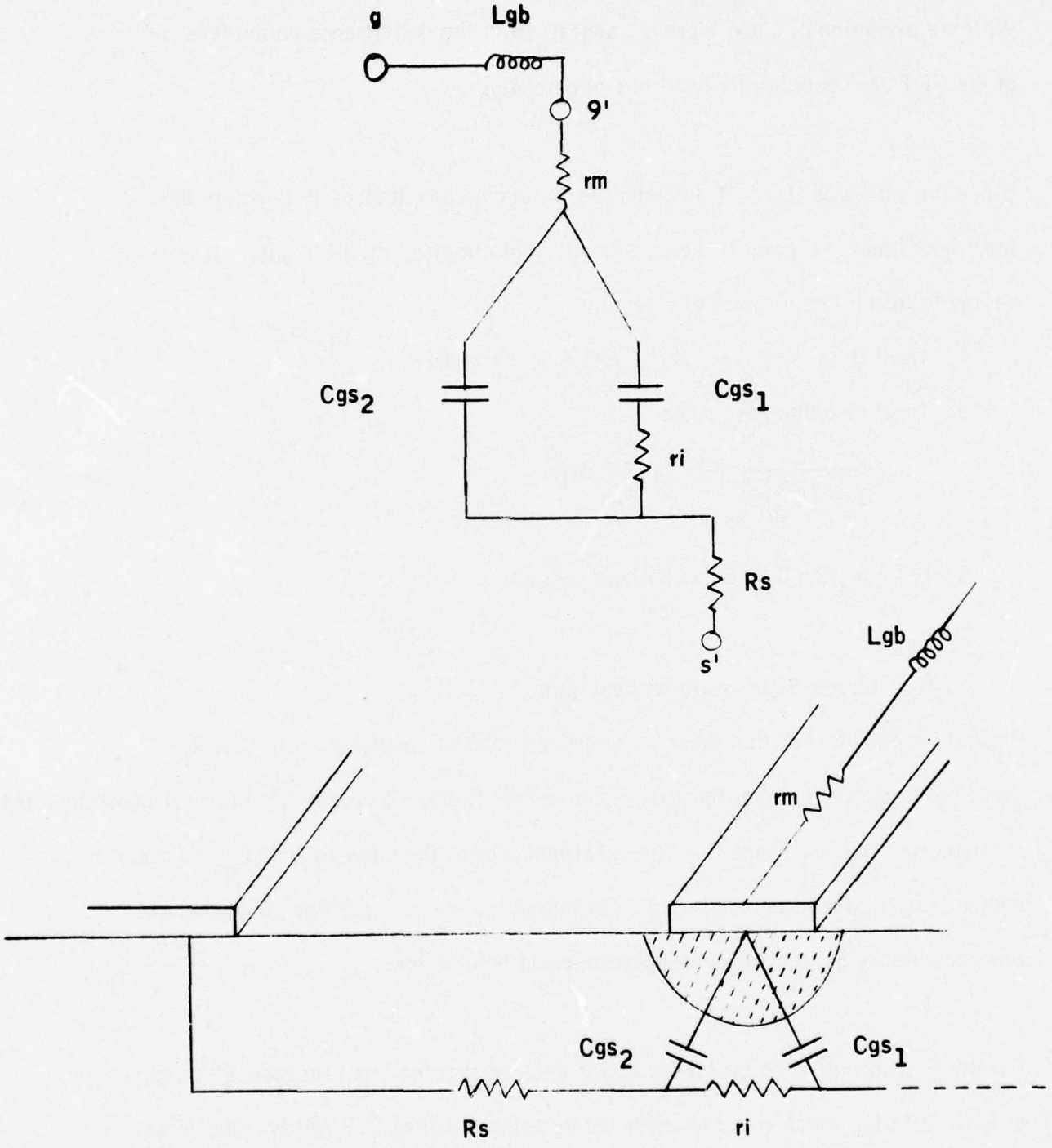
$$\frac{1}{2\pi\sqrt{L_{gb}C_{gs}}} > 18 \text{ GHz}$$

3. $f_T = g_m/2\pi C_{gs}$ be as high as possible
4. R_{in} be low as possible for best gain

Actually it can be seen that these requirements conflict somewhat, e.g. low R_{in} gives better gain but higher input Q. Requirement Number 3 is probably the most important, and it stipulates both low R and C. The question becomes then how low can C_{gs} be made without sacrificing other parameters. For example, a very small device would have low capacitance but the transconductance would also be low.

For the first iteration on the mask, it was decided that the input resonance should be at least 20 GHz which could be achieved by using a pair of 0.7 Mil bonding wires. A pair of widely spaced bonding wires has an inductance of $\sim$0.4 nhys.

Figure 1



EQUIVALENT GATE CIRCUIT

$$\therefore C_{gs} = \frac{1}{\omega_o^2 L_{bg}}$$

$$= \frac{1}{\left(2\pi \times 20 \times 10^9\right)^2 \left(.4 \times 10^{-9}\right)}$$

$$= 0.16 \text{ pf}$$

The parameter C_{gs} is a complex function of bias, size, and degree of velocity saturation. For a first order estimate a somewhat shortened expression for C_{gs} will be used:

$$C_{gs} \simeq \frac{\epsilon\epsilon_o L_g W_g}{a} \cdot \frac{4}{3} \cdot \left[\frac{1 - \beta/2}{(1 - 2/3\,\beta)^2}\right]$$

where

$$\beta = 1 - \left(\frac{V_g + \phi}{V_p + \phi}\right)^{1/2}$$

ϕ = 0.8 Volts

a = active (epitaxial) layer thickness

It will be necessary here to anticipate a later section and use the values of a = .15μ and Vp = 3.25V, and V_g = 2.5V for an operating current of 10 ma; then:

$$C_{gs} = 0.16 \times 10^{-2} = 4.74\, W_g \times 10^{-12}$$

$$W_g = 0.034 \text{ cm}$$

For the first mask a total gate width of 360 microns was used.

After the gate length and width are determined, it is necessary to decide on the general general topology of the device. First it should be recognized that a single gate 360 microns long would give an intolerable phase shift and loss between the gate pad and the end of the gate. Thus the gate must be broken up into n segments. This means that an

iterative design is needed. Figure 2 shows several possible designs for transistors with multiple gates. The last figure is a reproduction of that used in the proposal and forms the basis for the first FET design. To determine n, the number of gates, it is necessary to calculate the gate parameters using a transmission line model. The total capacitance is already known (.16 pf) and only the resistive loss and inductance are yet to be determined. Two types of gate metal were used in the contract, Cr/Pt/Au and Ti/W/Au. Since the Ti/W/Au system can be made with thicker gold, the sheet resistance is lower, e.g.:

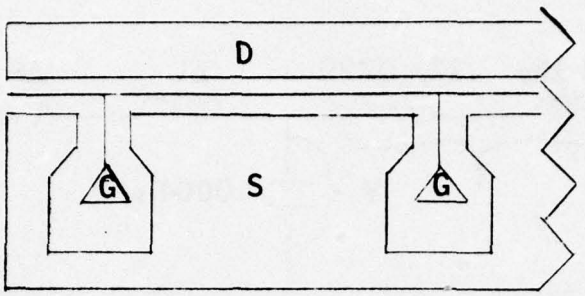
Table I

Gate Resistance, Lg = .5 μM

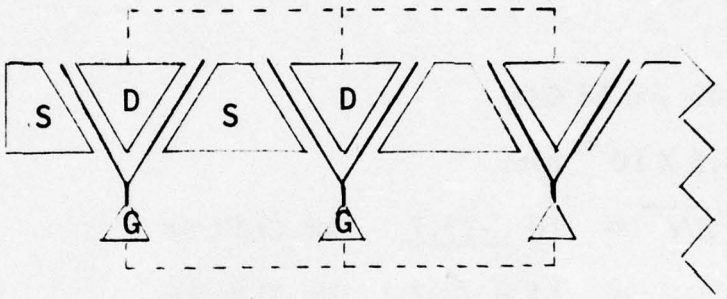
Gate Material	R_{Sheet}	t_{gold}	ΔR, Ω/micron
Cr/Pt/Au	.06 Ω/□	1μ	0.12 Ω
Ti/W/Au	.036 Ω/□	.5μ	0.072 Ω

The inductance of the gate is calculated from the equations for the limiting inductance of wires,[1] and is calculated to be 0.4 phy/micron. The difference in effective diameter for the two types of gate has a trivial effect on inductance although resistance is reduced about 40% for the thicker metal. With a total capacitance of 0.16 pf, the incremental capacitance, Δc is 0.16/360 = .0004 pf/micron. This leads to the gate model given in Figure 3. When compared with the model in the proposal for the 1 μM FET, it will be noted that the series resistance is higher due to the shorter gate length l_g. If the gate loss is to be kept under 1dB, then the maximum gate width must be limited to 40 microns. Since the values for C and L

Figure 2



A



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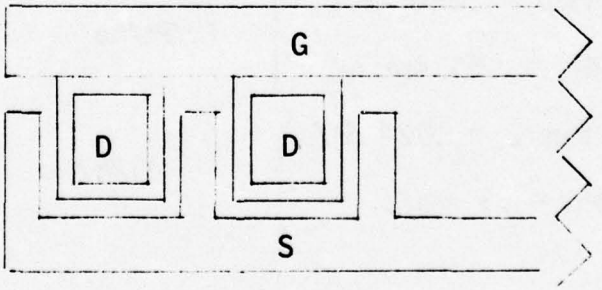
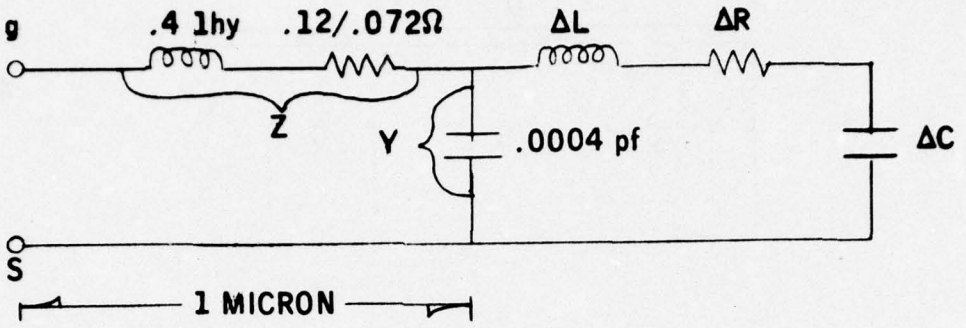


C

MULTIPLE GATE FETS

Figure 3



$j\omega \Delta L = .05$ at 18 GHz

$j\omega C = 4.5 \times 10^{-5}$ mhos

$Z_o = \sqrt{Z/Y} = 18 \angle -33.7$ for Cr/Pt/Au

$= 14.8 \angle -27.6$ for Ti/W/Au

$\gamma = \sqrt{ZY} = .007 \angle 56.3$ for Cr/Pt/Au

$= .006 \angle 62.4$ for Ti/W/Au

α = .003 nepers/μ ≅ .026 dB/μ
β = .0058 rad/μ = .33 deg./μ
} Cr/Pt/Au

α = .0028 nepers/μ = .024 dB/μ
β = .0053 rad/μ = .3 deg/μ
} Ti/W/Au

18 GHz Transmission Line Parameters

for Lg = .5 μM

calculated are somewhat on the high side, a gate width of 60 microns was used thus giving 6 gates for a 360 micron FET.

At this point it is necessary to determine the spacings between the gate and source, and the gate and drain. From a performance point of view, it is desirable to minimize the spacings; particularly the one between the source and gate which constitutes a part of R_s. The spacing between the gate and drain has a second order effect on performance. A decision was made to make the spacings 1 and 1.5 microns based on:

- Yields; in defining 1 micron spaces.
- Reliability; based on our ability to assure clean, non-shorting separation between source and gate.

The last step in obtaining the basic horizontal FET dimensions consists of selecting the geometry of the source and drain contacts. Large areas are easy to bond to and may have lower contact resistance. On the other hand, an unnecessarily large drain area can make output capacitance too high and reduce bandwidth. In addition, a very large device spread out over a very large area could cause unnecessary phase shift between the various drain areas. The minimum source or drain length (i.e. in the direction of current flow) can be calculated from the contact resistivity. (Source or drain width is the same numerically as gate width). In the proposal, experimental contact resistivities ρ_c of $1 - 5 \times 10^{-6}$ were reported. Although slightly lower values have been obtained from time to time, it is felt that this is now a good average range of values. Using an epi sheet resistance of 1000 ohm/$\square$ the contact resistance can be calculated.

$$R_{con} \simeq \frac{1}{Wg} \sqrt{R_s \rho_c} \cdot \text{Coth} \left[d\sqrt{\frac{R_s}{\rho_c}} \right]$$

d = Contact length

R_s = epi sheet resistance

ρ_c = Specific contact resistivity

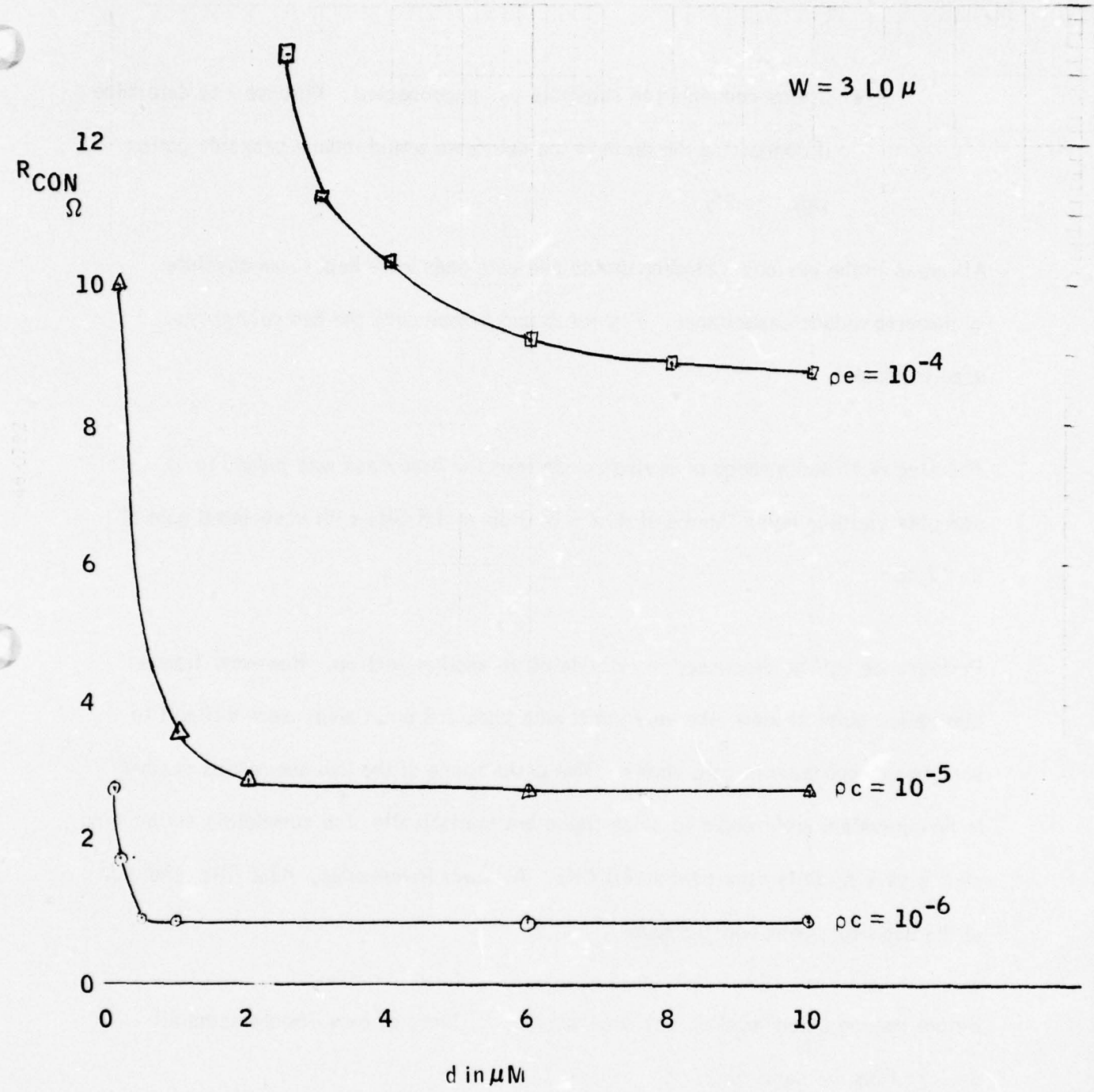
Wg = Gate or contact width

Figure 4 shows a plot of contact resistance versus d, the contact length. At the time the proposal was written it was not certain that a 10^{-6} ohm cm contact resistivity could be made consistently. With a better understanding of the role of epitaxy thickness, 5×10^{-6} is now close to the average value achieved. With this amount of contact resistivity, contact length ceases to be a design constraint, whereas with a contact resistivity of 10^{-4}, designs were limited to lengths greater than 10 microns. (Refer to Figure 4)

The proposal indicated that at least two mask layouts would be evaluated before the final FET design was selected. It was decided that the first design should be experimental, in order that several questions could be answered. Thus the mask included the following tests:

- Completely surrounding source metal vs. semi-surrounding. Purpose - to determine if common lead inductance could be reduced by this technique.
- Separate vs. joined gates. Purpose - to determine if the additional parasitic capacitance from a larger gate pad would reduce performance significantly.

Figure 4



Contact Resistance vs. Contact Length (d)

R sheet for Epi $\simeq$ 1000 Ω/

- Drains connected to substrate vs. unconnected. Purpose - to determine if connecting the drain to the substrate would reduce backside gating significantly.

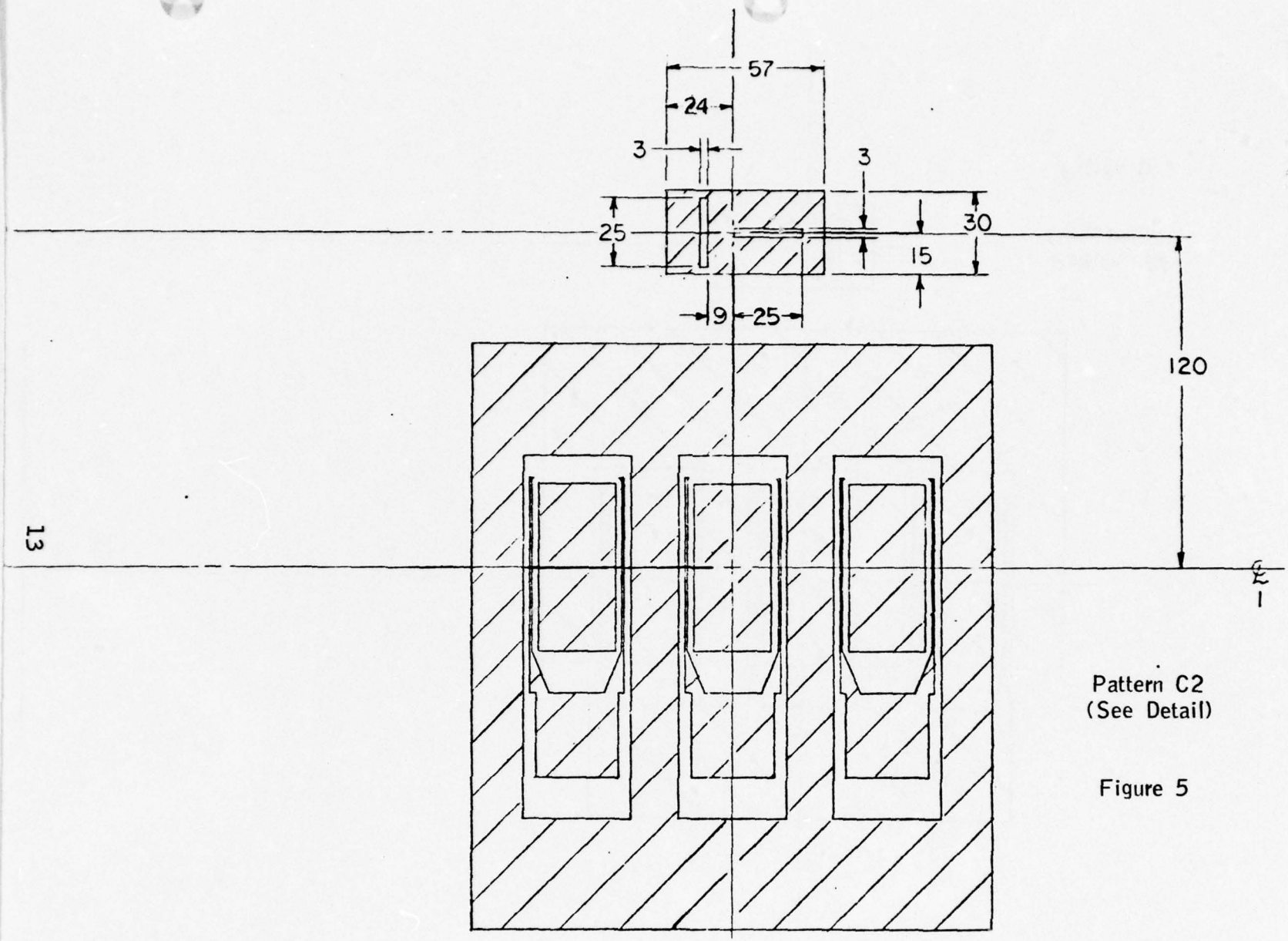
All areas in the devices including drains and gate pads were kept to an absolute minimum to reduce capacitance. Figures 5 and 6 reproduce the two geometries used in Mask I.

The electrical performance of devices made from the first mask was judged to be adequate yielding noise figures of 4.2 - 5.0 dB at 18 GHz with associated gain of 5 - 7 dB.

Performance will be discussed in more detail in another section. However, from a fabrication point of view, the very small gate pads and drain areas were difficult to bond to without drain to gate shorts. The performance of the two geometries seemed to be equivalent with regard to noise figure but statistically, the completely surrounding source gave slightly more gain at 18 GHz. At lower frequencies, <12 GHz, the gain of the two geometries was the same.

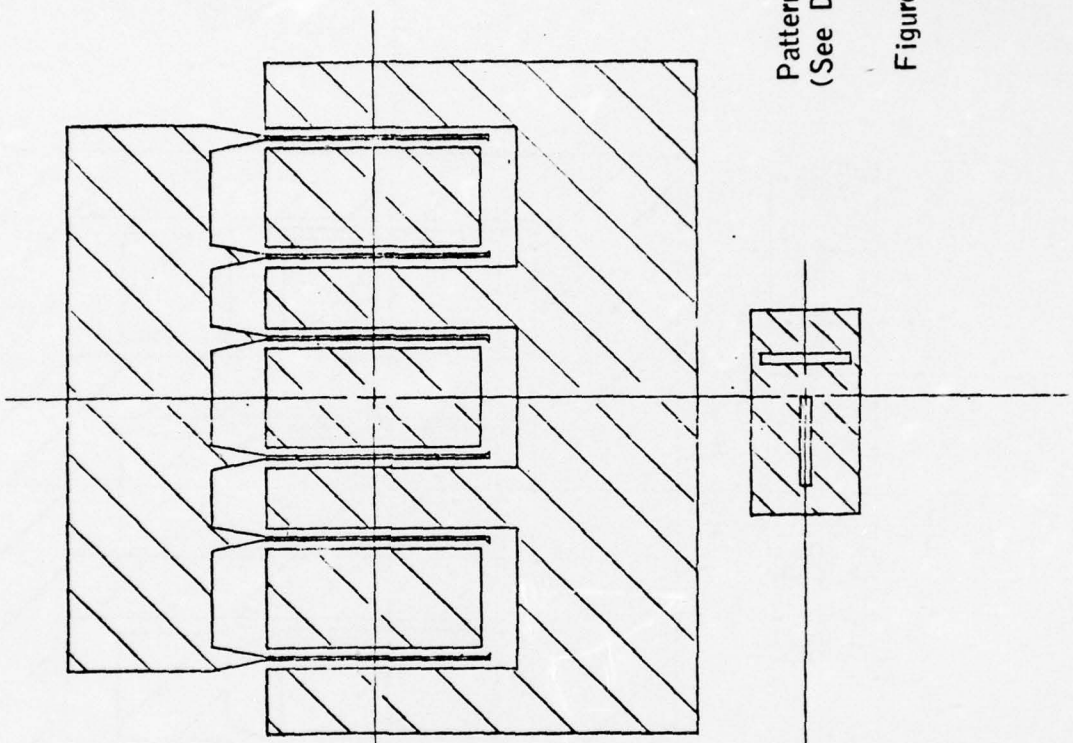
Before making a new mask it was necessary to conduct two experiments using all devices from the same run.

- Separate vs. joined gates. Previous data was ambiguous and gave conflicting results.
- Alternate vs. adjoining sites.



Pattern C2
(See Detail)

Figure 5



Pattern CI
(See Detail)

Figure 6

The second test was needed to determine whether or not a new mask design with expanded spacing between the drains would result in a phase error which would reduce gain. Figure 7 shows the two bonding schemes used for the second test. Since only two of the three sites are used, the devices used in the test exhibited Idss and g_m values 2/3 of those obtained with completed devices. It was also noted that noise figures optimized at roughly 2/3 the usual optimum current (i.e. 7 mA vs. 10 mA). The results of both tests were negative except possibly that the surrounding source gave more gain at 18 GHz.

On the basis of these results, a new mask was drawn up using:

- Wider spacing between the three drain centers to make bonding easier.
- Larger more widely spaced but interconnected gate bonding pads.

Mask number II is shown in Figure 8. At the conclusion of the first phase of the contract, several runs had been made using the new mask. Bondability and yield had been improved markedly and performance did not suffer as a result of the changes.

c. Vertical Geometry: The vertical geometry of a FET is physically the least apparent but can have the most profound effect on transistor performance. Starting substrates of semi-insulating GaAs can influence the constitution of succeeding layers in a manner which is not yet clearly understood. For example; poor mobility, backside gating, assymetry, Gunn oscillation, and other effects are related to the substrate itself. To date, no clearcut way of segregating "good" vs. "bad" substrates has been found. Heating substrates to a predetermined high temperature and then checking for conductivity

Figure 7

SITE SPACING EXPERIMENT

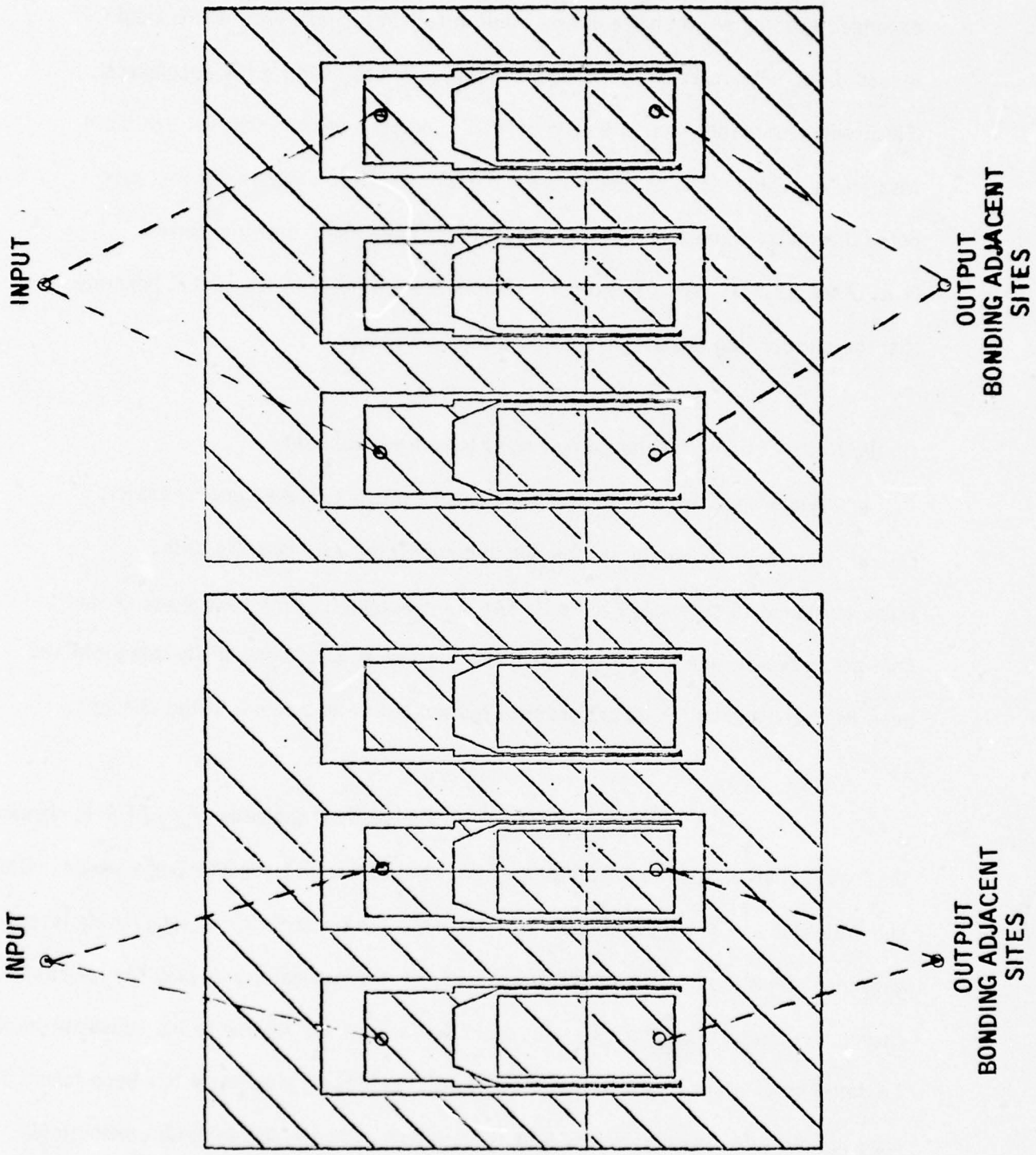
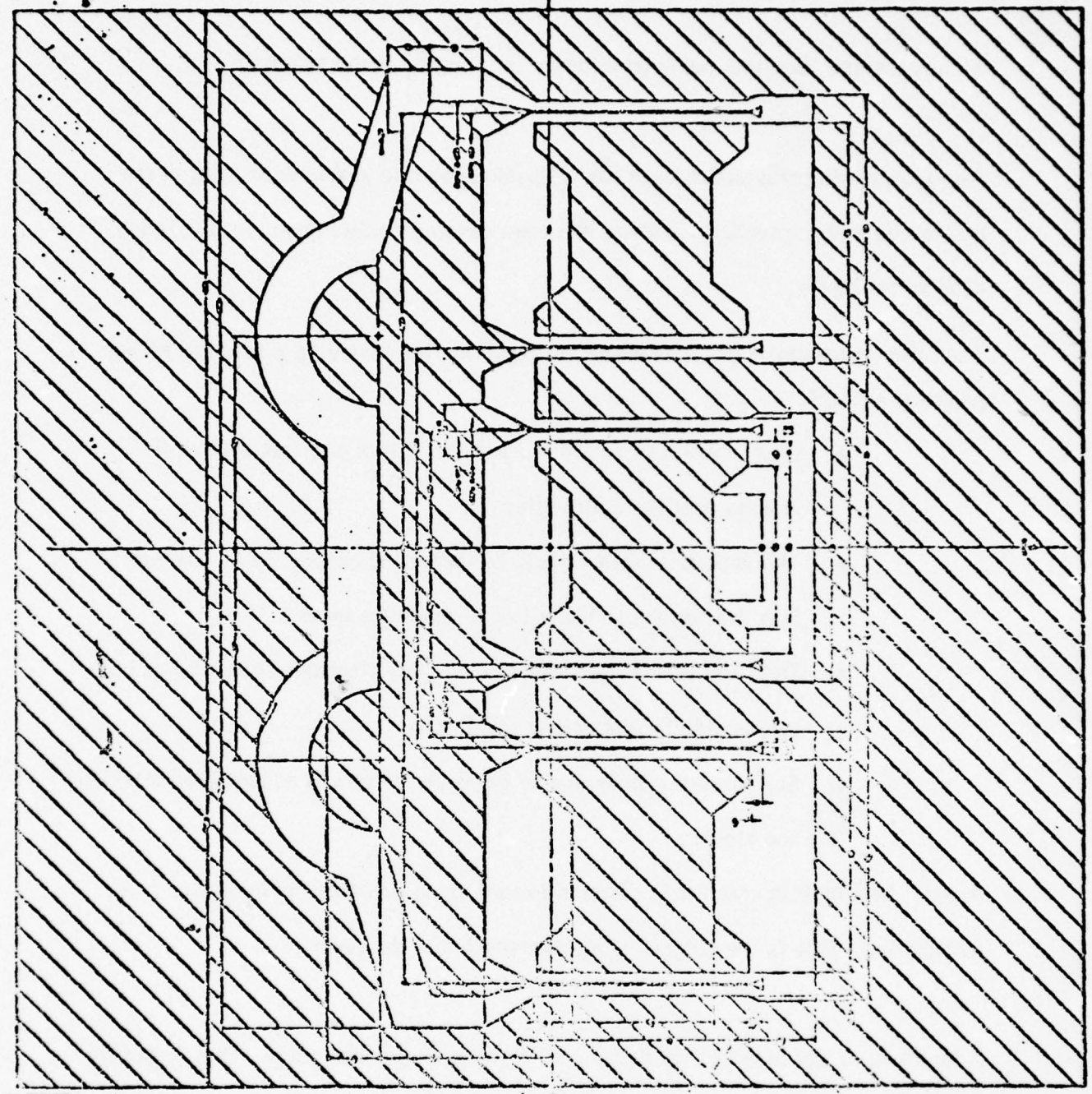


Figure 8



0.5 μM Mask No. 2

eliminates one, but only one type of defect originating in the substrate.

The introduction of a buffer layer can alleviate substrate problems to some degree and to this end a considerable effort has been devoted on this contract to building good buffer layers.

The following material considerations are important for achieving a suitable active layer for an FET.

- Layer thickness control should result in a constant pinch-off voltage over the entire slice.
- The impurity profile should be controlled accurately all the way from the surface to the buffer or substrate layer.
- The mobility and saturation velocity of electrons should be as high as possible for the doping level used.
- Surface morphology should be nearly perfect to assure good masking and yield.

A major task on this contract is directed toward using implantation for active layer fabrication. This is the subject of a major section of the report.

A fourth layer can also be added to the FET to improve performance. This is the N+ layer. If an FET does not have an N+ layer under the contacts, the impurity level in the channel is a compromise between the low contact resistance obtained with high doping levels and the high mobility and carrier velocity obtained with lower doping levels.

An implanted N+ layer was attempted but was not successfully fabricated because of the reasons given in the section on implantation.

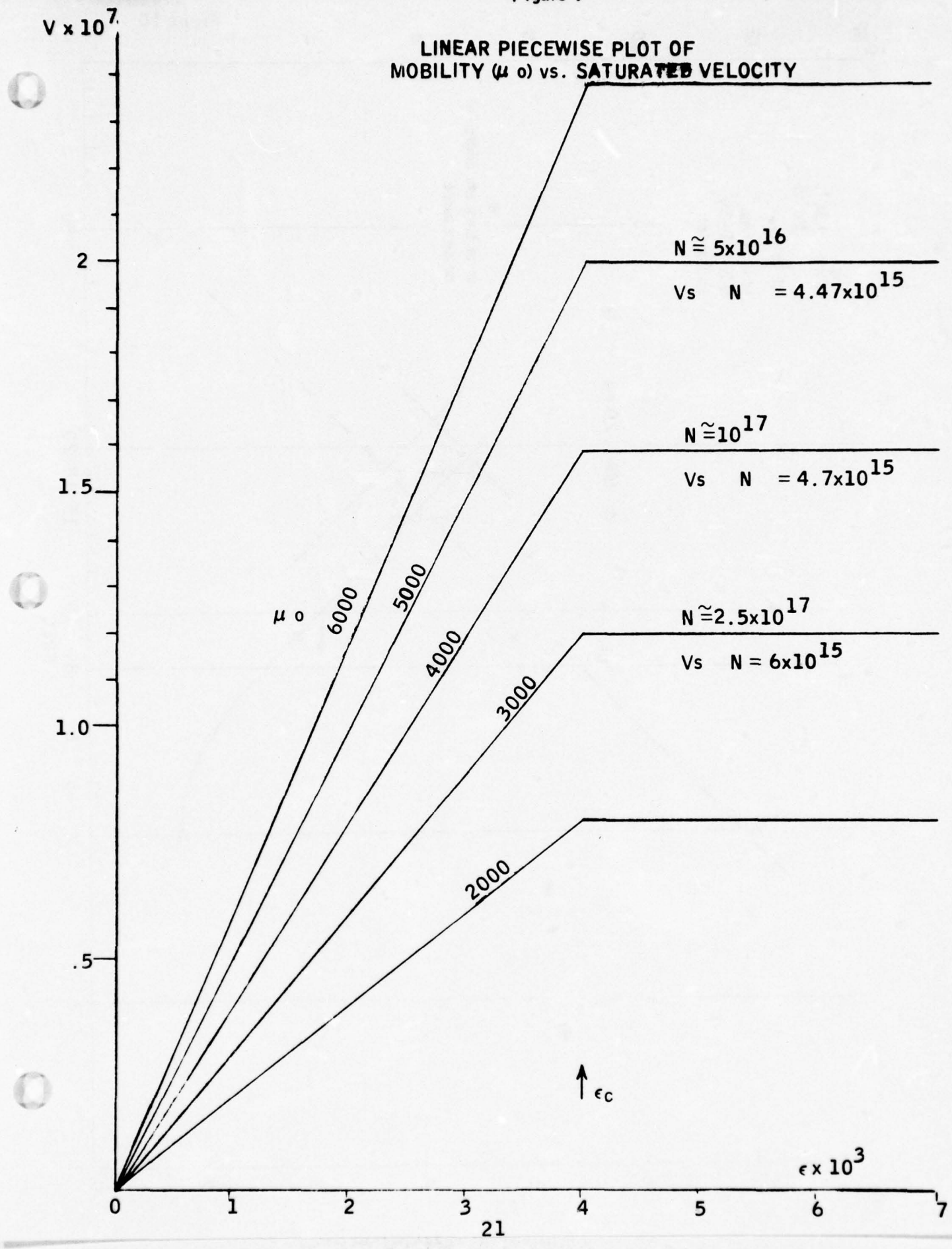
The active layer for the devices delivered in the first phase was grown by the LPE process. Layer thicknesses ranging from 0.12 to 0.2 microns were used with corresponding impurity levels ranging from 2.5×10^{17} down to 1.0×10^{17}. It is known both from theoretical calculations and from experimental data that as the gate length is reduced, the thickness of the epitaxial region must also be reduced. When the active region is made thinner it also must be doped more heavily in order to maintain conductivity which affects transconductance, etc. For a 0.5 micron gate, the optimum material thickness is close to 0.15 microns with a corresponding doping level in the channel of 1.5×10^{17}. The resulting pinch-off potential is approximately 2.50 Volts.

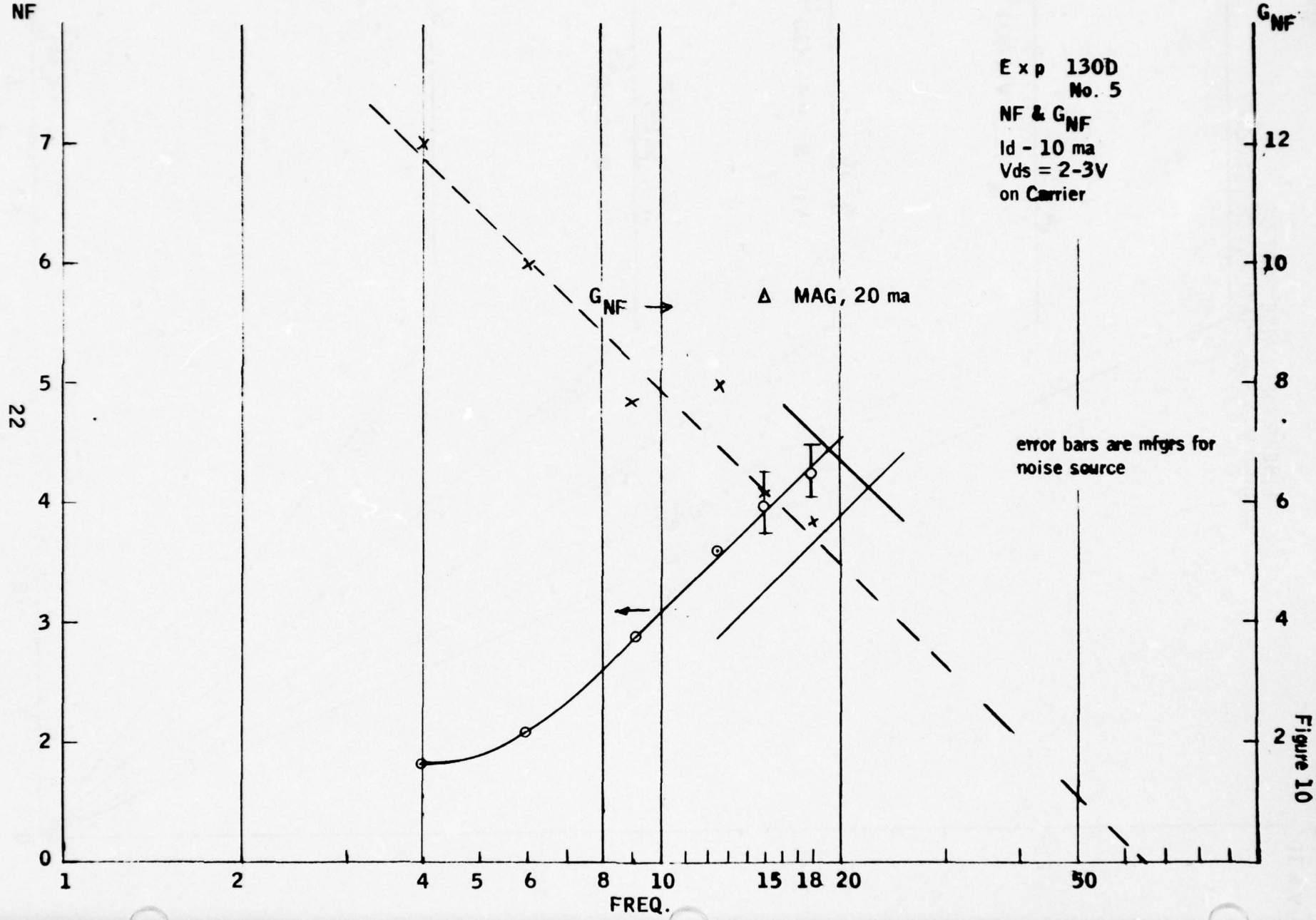
Since both g_m and C_{gs} are proportional to $\sqrt{N}$, it would be expected that f_t would be invariant with N. It was found that higher doping level in the channel did indeed reduce contact resistance and increase low frequency g_m. However, the high frequency value of g_m was not increased in the same proportion that C_{gs} was, with the result that f_t was lowered. One possible explanation for this is that the higher doping level reduced V_s, the saturated velocity of electrons. It appears that the present theory which predicts transconductance as proportional to $V_s \times \sqrt{N}$, may be inadequate.

It is also possible that the relationship between V_s, N, and μ_o are not explained properly by present theory. Figure 9 summarizes the relationship as presently accepted. Best performance to date for devices built without N+ layers came from epitaxial material doped to about 1.5×10^{17} atoms/cm^3. Phase II may permit gathering sufficient data to clarify these ambiguities.

d. FET Performance: This section will review the performance achieved by the FET's and relate the measured parameters to an equivalent circuit. Noise performance will also be discussed. Data on S parameters will be found in the section on amplifier design.

(i) Noise Performance. The proposal set forth as an objective a noise figure of 4-5 dB with 10 dB associated gain at 18 GHz. A number of runs have met the noise figure objective, but the gain has been somewhat less than expected with the best runs giving only 8 dB gain at best noise figure source admittance. Performance of one of the better runs is shown in Figure 10. The lower than expected gain has had the effect of increasing the amplifier noise figure so that the objective was not met. Difficulties in maintaining high mobility in the active layer, particularly near the interface with the substrate or buffer layer, has resulted in a lower transconductance than is needed to meet the contract objective. The section on materials discusses this problem in detail.


V x 10^7
LINEAR PIECEWISE PLOT OF
MOBILITY (μ o) vs. SATURATED VELOCITY
N ≅ 5x10^16
Vs N = 4.47x10^15
N ≅ 10^17
Vs N = 4.7x10^15
N ≅ 2.5x10^17
Vs N = 6x10^15
μ o
6000
5000
4000
3000
2000
2
1.5
1.0
.5
ε_c
ε x 10^3
0
1
2
3
4
5
6
7

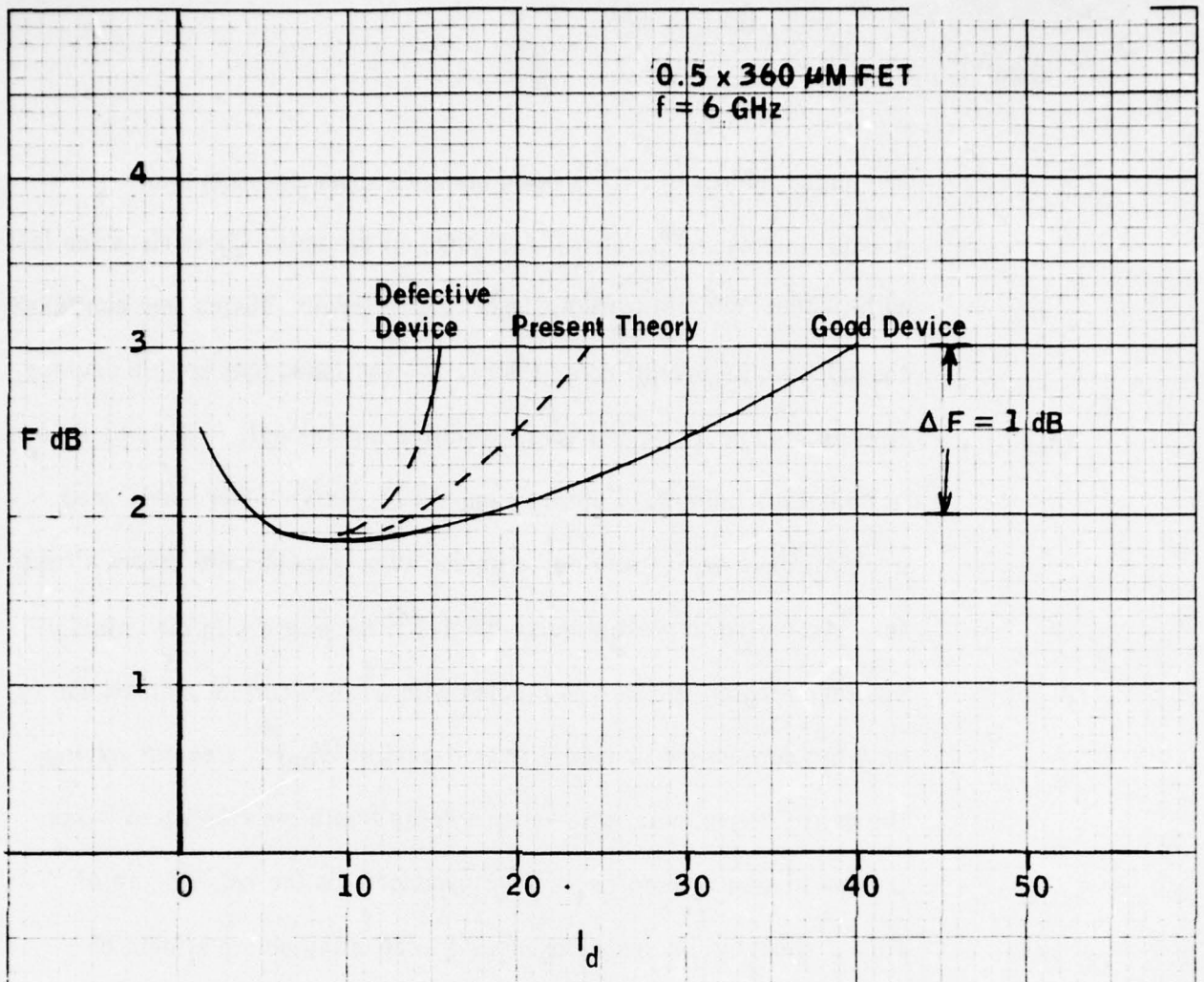


Avantek inc.
Figure 10

The noise figures of FET's drain currents above optimum is of special interest to the circuit designer. If the noise figure rises too fast with increasing drain current, later, higher power, stages may contribute too much to the overall noise figure. It was found that certain devices (related to specific substrates) exhibited anomolously high noise figures at high drain current. Refer to Figure 11. On the other hand, good devices gave much lower noise figures than present noise theory allows for. According to present noise theory[2] the carriers in the velocity saturation region diffuse as dipoles with a noise current proportional to dc drain current and inversely proportional to $(V_{sat})^3$. Devices having the defective characteristics shown in the figure are eliminated in our present screening process. Continued work on the noise figure of FET's should yield some very useful information on the effects of current levels.

(ii) Model. Data for the model to be presented was obtained from:

- S parameters
- dc data
- Curve tracer
- 1 MHz capacitance
- 1 KHz data
- Calculations



FET
Noise Figure vs. Drain Current

Figure 12 and the accompanying Table II summarize the results of the modeling. Not all of the parameters can be cross checked by more than one method. The values shown represent a composite average from a number of runs.

2. FET Process Development

Process development for the 0.5 micron gate length device was on an evolutionary basis. This approach was chosen to insure the availability of interim devices for amplifier circuit design and to maximize the probability of the success in a short time schedule. Therefore, the initial approach was to reduce the gate length of our standard 1.0 micron FET design (see Figure 13).

This reduction in gate length was accomplished by the use of a 0.75 micron mask set. The mask set utilized chrome masters obtained directly from the step and repeat camera. Gate lengths of 0.75 to 0.85 microns were obtained with relative ease. However, our standard process for FET fabrication utilizes a lift technique for the gate definition, thus, the steepness of the edge of the resist is of paramount importance. The angle at the edge of the resist exposed with this mask was typically 70° to 80° instead of the desired 90° angle. This leads to "strings" of gate metallization. Metallization which was evaporated onto the edge of the resist often attached to portions of the 500 micron gate lines. The application of poly-crystalline gallium arsenide (PGA) over the gate channel stabilized the positions of these metal fragments. However, visual examination under 1250X microscope magnification was used extensively to eliminate the questionable die.

Model for 1/2 μ M FET

Figure 12

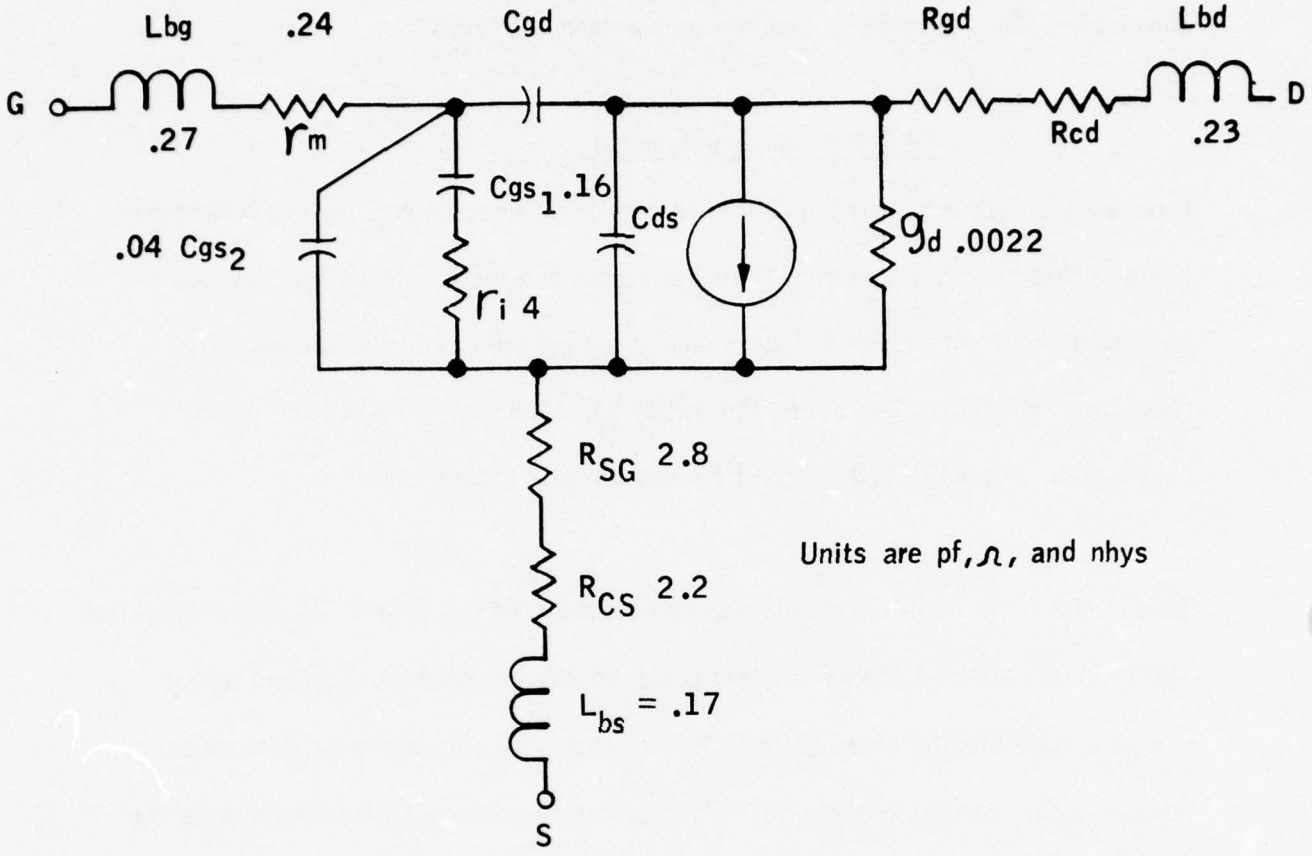


Table II

1. $r_m \cong \frac{1}{6}\left[\frac{1}{3} R_{SHM} \cdot \frac{Wg}{Lg}\right] = \frac{1}{6}\left[\frac{1}{3} .036 \frac{60}{.5}\right] = .24$ CAL

2. $R_{SG} + R_{SG} = 5\Omega$; Curve Tracer

3. $R_{SG} = R_{SH} \times S_{sg}/W_g = 1000 \times 1/360 = 2.8\Omega$ CAL

4. $R_{CS} = 5 - 2.8 = 2.2\Omega$
   Check $R_{CS} = \frac{1}{W} \cdot \sqrt{RsPc}$; $Pc = 6 \times 10^{-6}$

5. $R_{GD} = 1.5 \times R_{SG} = 4.2\Omega$ CAL

Table II (cont.)

6. $Cgs_1 + Cgs_2$ ^{2} .20 pf, from Cgs vs Vgs

7. Cgs_2 = .04 pf, from depleted channel cap.

8. Cgs_1 = .16 pf ; Step 6-7

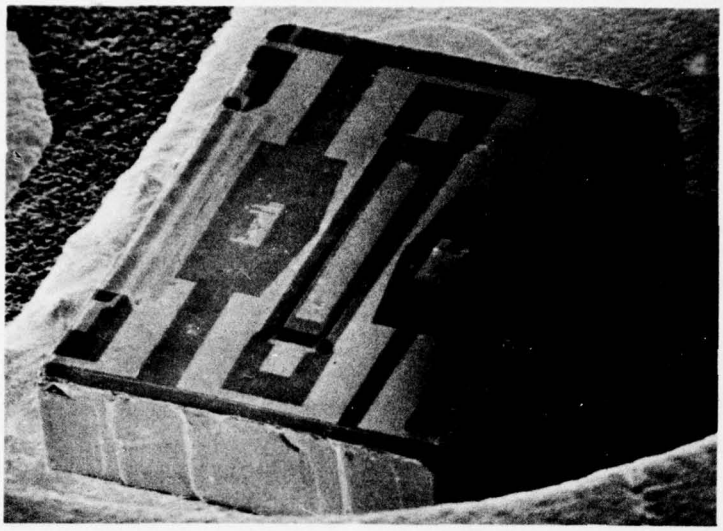
9. $R_{CD} \cong Res \cong 2.2$

10. $r_i = R_{GSO} - (r_m + R_{SG} + Res)$
$= 9 - (.24 + 2.8 + 2.2) \cong 4\Omega$

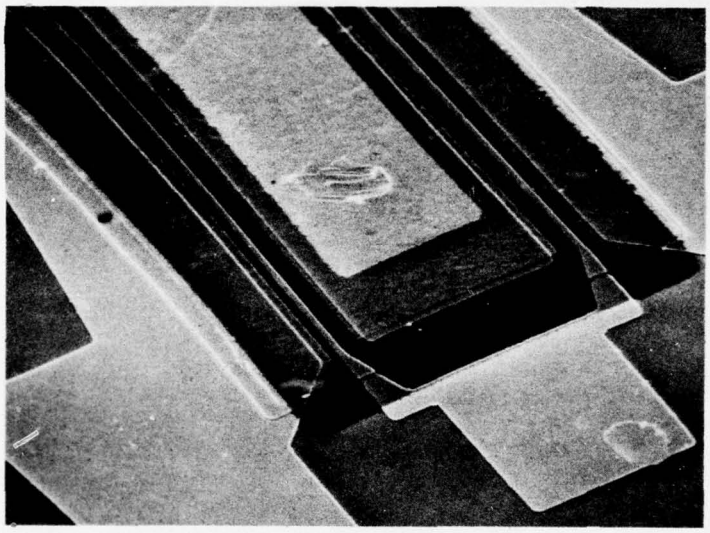
11. $g_{mo} = \frac{g_{mo\ term}}{1 - g_{mot}(R_{SG} + Res)} = \frac{.032}{1 - .032\ (5)} = .038$ mhos ; Curve Tr. and CAL

12. $\tau = 2\pi\ Cgs_i = 2\pi(.2 \times 10^{-12} \times 4)$
$= 5 \times 10^{-12}$
$= 5$ ps
$= 4$ ps from S parameters

13. Cds = .05 - .07 (S par)



Avantek M-100 1 μM Geometry



Avantek M-100 1 μM Geometry

Figure 13

The first 0.5 micron R&D mask set arrived with gate dimensions of 0.5 to 0.6 microns. The problem with this mask set was the poor layer to layer registration of the gate mask with the ohmic contact pattern of the previous mask level. Only a handful of devices were obtained from each gallium arsenide slice. A second R&D 0.5 micron set was provided by the mask vendor, and this set did meet the layer to layer registration specification.

The process difficulties encountered with this second, 0.5 micron, R&D mask set were similar to those of the specially selected 1.0 micron mask set. That is, metal string problems often appeared whenever the exposure and development of the resist yielded an accurate 0.5 micron gate. However, the metal strings problem was within a workable tolerance. Good 0.5 micron devices were fabricated from this mask set for the initial 7-15 GHz amplifier designs.

The desire to reduce gate metallization resistance lead us to explore the "etch back" technique. Our standard gate metallization with a platinum Schottky barrier is not adaptable to an etch back process since it is difficult to etch platinum without damaging the gallium arsenide epitaxial layer. Thus, several other Schottky barrier metals were considered. A mixture of titanium tungsten (Ti-W 10%) was chosen over pure tungsten due to its superior adhesion properties. The titanium tungsten mixture has well defined chemical etchability properties and in addition Avantek has suitable deposition equipment for this mixture. The "etch back" process requires masks of the same sophistication as the lift process to define the 0.5 micron gate. However, the etch back process can produce

gate thicknesses up to 1.25 microns with line widths of 0.5 microns, moreover, metal strings do not exist. We are using the etch back process to fabricate most of our 0.5 micron FET's at this time.

B. Materials Development

1. Introduction

The effort on this contract pertaining to materials can be divided roughly into two general areas. The first utilizes liquid phase epitaxy (LPE) and is directed toward:

- Material Improvement - higher mobility (μ_0), higher saturated velocity (V_s), better surface morphology, etc., all in the active layer.

- Buffer layer development - development of a process producing buffer layers which will alleviate or reduce problems associated with the substrate as it affects the active layer. Improvement of mobility in the active layer can also be expected from a good buffer layer.

The second area of effort is directed toward the use of implantation to achieve both N+ contact layers and N-type active layers. Efforts to form an N+ layer were not successful as explained in the next section. The implantation of selenium into buffer layers to form an implanted active layer produced working FET's, although the characteristics were not as good as FET's on epitaxial layers.

2. Buffer Layer Growth, LPE

In this section, the growth of a buffer layer on semi-insulating substrates using liquid phase epitaxy is discussed.

The advantages resulting from the incorporation of a buffer layer are several:

- Prevention of substrate impurities from moving into the active layer.
- Prevention of electrical trapping effects from affecting the active layer.
- Providing a damage free, single crystal, surface on which to grow the very thin active layer.

The first of these advantages means that the mobility in the active layer will be higher. Figure 14 gives some approximate relative mobilities for active layers with and without a buffer. In addition, further tests have shown that more of the dopant remains active near the active layer/buffer interface than near the active layer/substrate interface.

The advantages listed above imply a number of desirable changes in the characteristic of the FET after incorporating the buffer:

- Very little or no looping
- No back side gating
- No breakup
- Reduction or elimination of Gunn oscillations

Finally, a damage free surface means that the active layer surface itself should be more nearly free from defects. A smooth final surface is also a necessity for uniform pinch-off and trouble free masking.

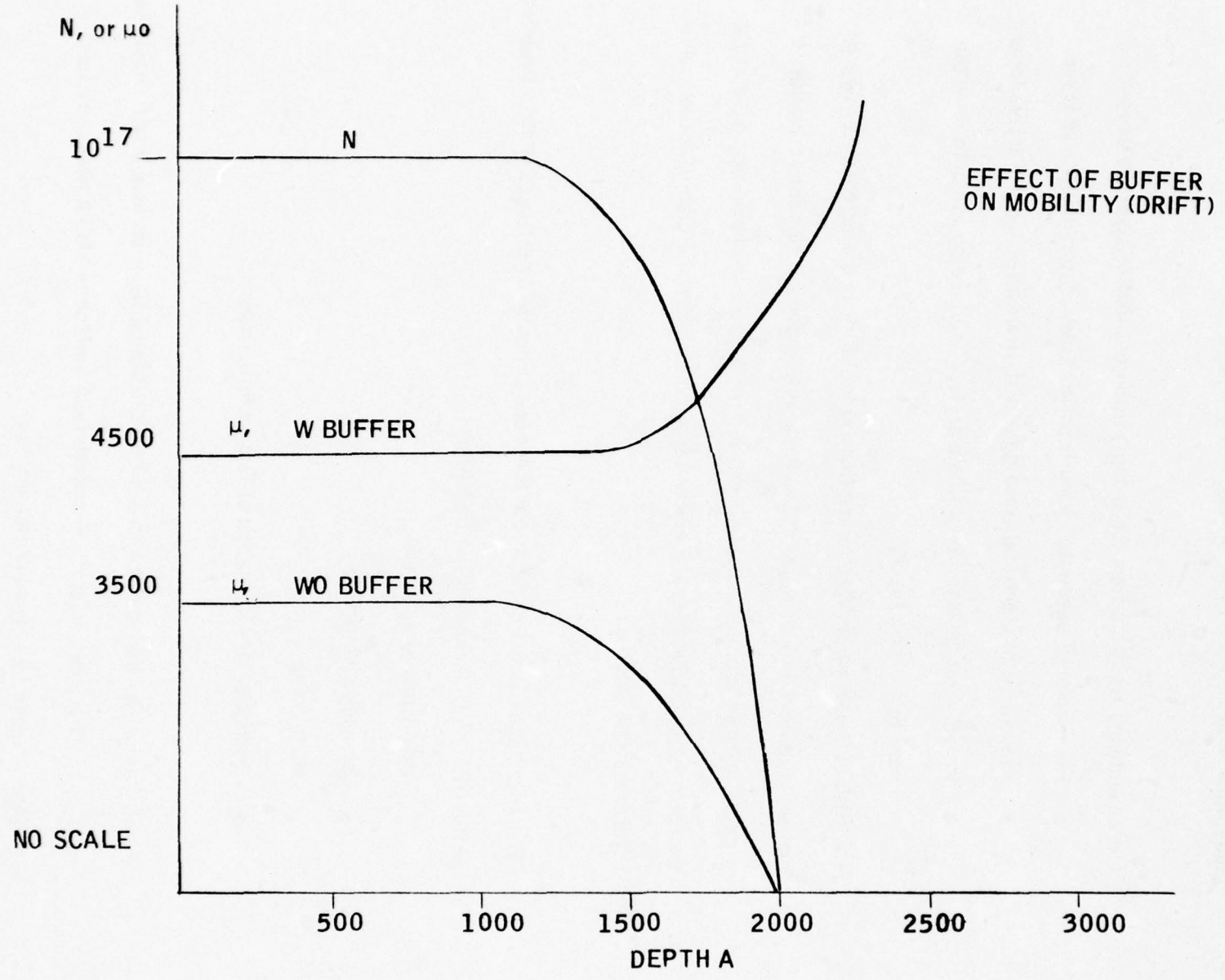


Figure 14 Avantek inc.

Very often when growing layers, poor wetting occurs with the result that the "scrape" to terminate the layer growth gives a wavey or convex surface. Problems such as these do not lend themselves to a detailed analysis, and no two formulas for layer growth are exactly the same.

One of the more successful buffer experiments (similar to that reported by Mattes et al [4]) carried out at Avantek showed that it was possible to make reproducible buffer layers with doping equal approximately to 10^{13} atoms cm^{-3}, N type. It was also found that P type layers doped to 10^{14} atoms cm^{-3}, $\mu_{RT} = 250\ cm^2/V\text{-sec}$ could be grown. Both N and P type buffers have been used as bases for growth of good active layers. P type buffers are subject to severe backside gating effects, however.

The Hall mobilities for N type ($\approx 10^{14}$) buffers are 7500 and 45,000 $cm^2/V\text{-sec}$ at 300°K and 77°K respectively. This ratio, 6:1, suggests a fairly high compensation level. It is possible that this compensation takes place during the period when the melt is baked out. A cooperative effort with Stanford University is directed toward the solution of this problem.

Another problem we have encountered is that of leftover melt after the scrape which causes some areas in the final surface to be thicker than others. This has been partially resolved by changing over to a new boat design which allows a much better fit between the slider and the boat floor. Although we have not been able to completely solve all of the problems associated with the buffer layer growth, considerable progress has been made and good buffer layers have exhibited the expected desirable characteristics

in FET's. Work will continue in this direction and will be directed to:

- Better yield
- Better surface morphology
- Better mobility with less compensation.

3. Implantation

a. Contact Improvement:

(i) Ion Implant. Two requirements for low resistance ohmic contacts are:

- High surface concentration at the semiconductor/metal contact interface
- High conductivity of the semiconductor underneath the metal contact.

The first requirement is necessary in order to achieve low specific contact resistance between the contact and semiconductor, whereas the second requirement minimizes the resistance which occurs as a result of the planar structure of the FET contact system.

Ion implantation of impurities such as Te , Se, and S provide a good solution to these requirements in the GaAs FET contact system. It should be pointed out that the requirement for high conductivity of the material under the contact means not only high doping concentration, but also high mobility, since the conductivity involves their product.

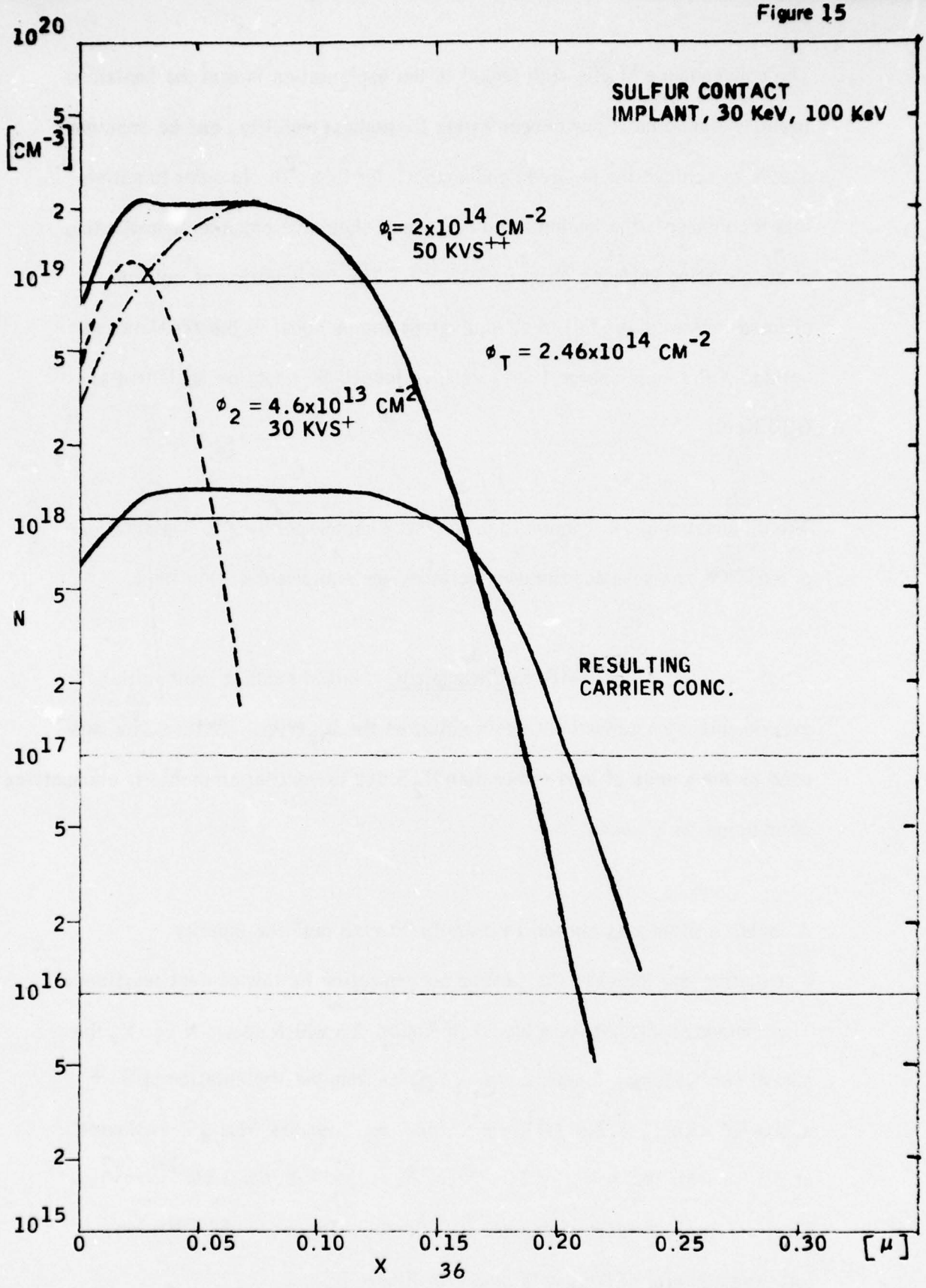
The consequence of this with regard to ion implantation is that the implanted impurity should have low concentration for highest mobility, and be implanted deeply to achieve the desired conductance, (or Qcm^{-2}). In order to satisfy this requirement, the implantation equipment should be capable of implanting at accelerating voltages of up to 300 KV. The implantation of multiple charged ions would result in an equivalent energy equal to the accelerating voltage X the ionic charge (i.e., doubly charged S could be implanted at 600 Kev).

The discussion of ion implantation work at Avantek pertains to implantations of ~60 KV maximum accelerating voltage, the equipment design limit.

(ii) Sulfur Implant. Initial contact implantation experiments were carried out using sulfur as the impurity. Solid sulfur was used as the source of ions rather than H_2S due to ventilation problems encountered when using toxic gases.

A double implant was chosen in order to "flatten out" the inpurity distribution and increase the surface concentration for low contact resistance. The implant conditions were based on Figure 15 which shows N vs X, the sum of two Gaussian distributions; ϕ_1 results from the implantation of S++ at 50 KV with $\phi_1 = 2 \times 10^{14} cm^{-2}$, and ϕ_2 results from S^+ implanted at 30 KV with $\phi_2 = 4.6 \times 10^{13} cm^{-2}$. $\phi_T = 2.46 \times 10^{14} cm^{-2}$. Considering the effects of degeneracy, doping efficiency, and diffusion, the expected plot of N vs X is shown in Figure 15.

Figure 15


SULFUR CONTACT
IMPLANT, 30 KeV, 100 KeV
$\phi_1 = 2\times10^{14}$ CM^{-2}
50 KVS^{++}
$\phi_T = 2.46\times10^{14}$ CM^{-2}
$\phi_2 = 4.6\times10^{13}$ CM^{-2}
30 KVS^{+}
RESULTING
CARRIER CONC.
[CM^{-3}]
N
10^{20}
5
2
10^{19}
5
2
10^{18}
5
2
10^{17}
5
2
10^{16}
5
2
10^{15}
0
0.05
0.10
0.15
0.20
0.25
0.30
[μ]
X

Implantation of sulfur was carried out according to this schedule using Cr doped substrates. Substrate temperature was maintained at 300°C during the implant. The implanted substrates were coated with a 1000Å film of Si_3N_4 (low temperature plasma deposited) and annealed at 750°C for 1/2 hour. Following the annealing step, the Si_3N_4 was removed, and the implanted layer evaluated using a JAC impurity profiler. Capacitance measurements of sulfur implanted layers in Cr substates indicated no electrical activity. The implantation was carried out again implanting into epitaxial layers rather than the bare Cr doped substrate.

Figure 16 shows the result of a sulfur implant carried out under the conditions just described. The starting material is an N-type epitaxial film grown on a Cr doped substrate. The maximum doping in the epitaxial film was $7 \times 10^{16}_{cm^{-3}}$, as indicated in the figure. The curve to the right of the figure was obtained after implantation and anneal. There appears to be only a displacement of the original profile, but no additional doping above that of the original epitaxial film. Similar behavior is seen in Figure 17. In this sample, an epitaxial film of $10^{17}_{cm^{-3}}$ doping was used. The plot to the right shows similar behavior to that of Figure 16; a displacement toward larger X but no increase in the carrier concentration. Reductions in the implantation dose were tried using values of $2.5 \times 10^{13}_{cm^{-2}}$ and $2.5 \times 10^{12}_{cm^{-2}}$. These lower

Figure 16

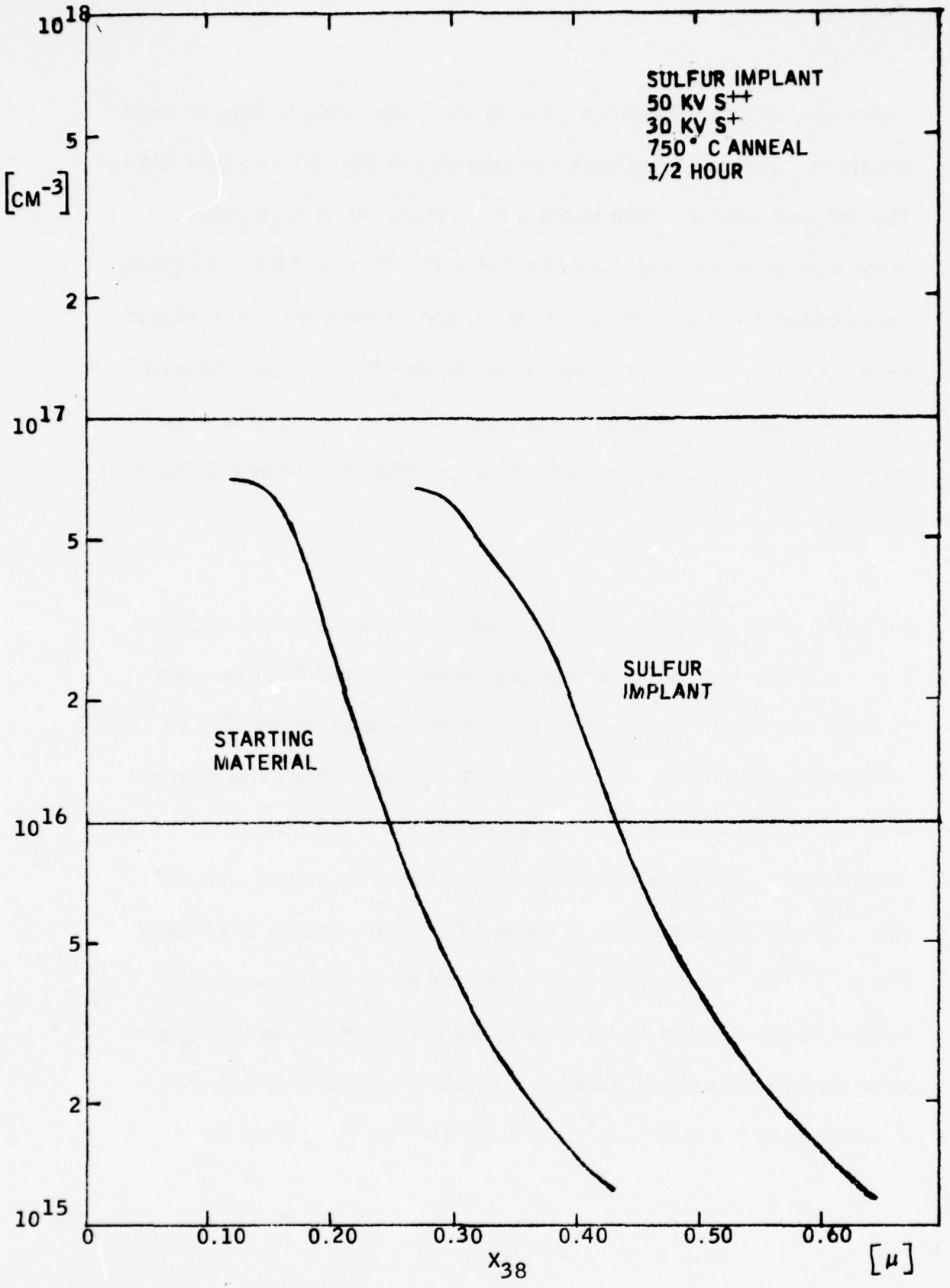

SULFUR IMPLANT
50 KV S++
30 KV S+
750° C ANNEAL
1/2 HOUR
[CM-3]
10^18
5
2
10^17
5
2
10^16
5
2
10^15
STARTING MATERIAL
SULFUR IMPLANT
0
0.10
0.20
0.30
0.40
0.50
0.60
X38
[μ]

Figure 17

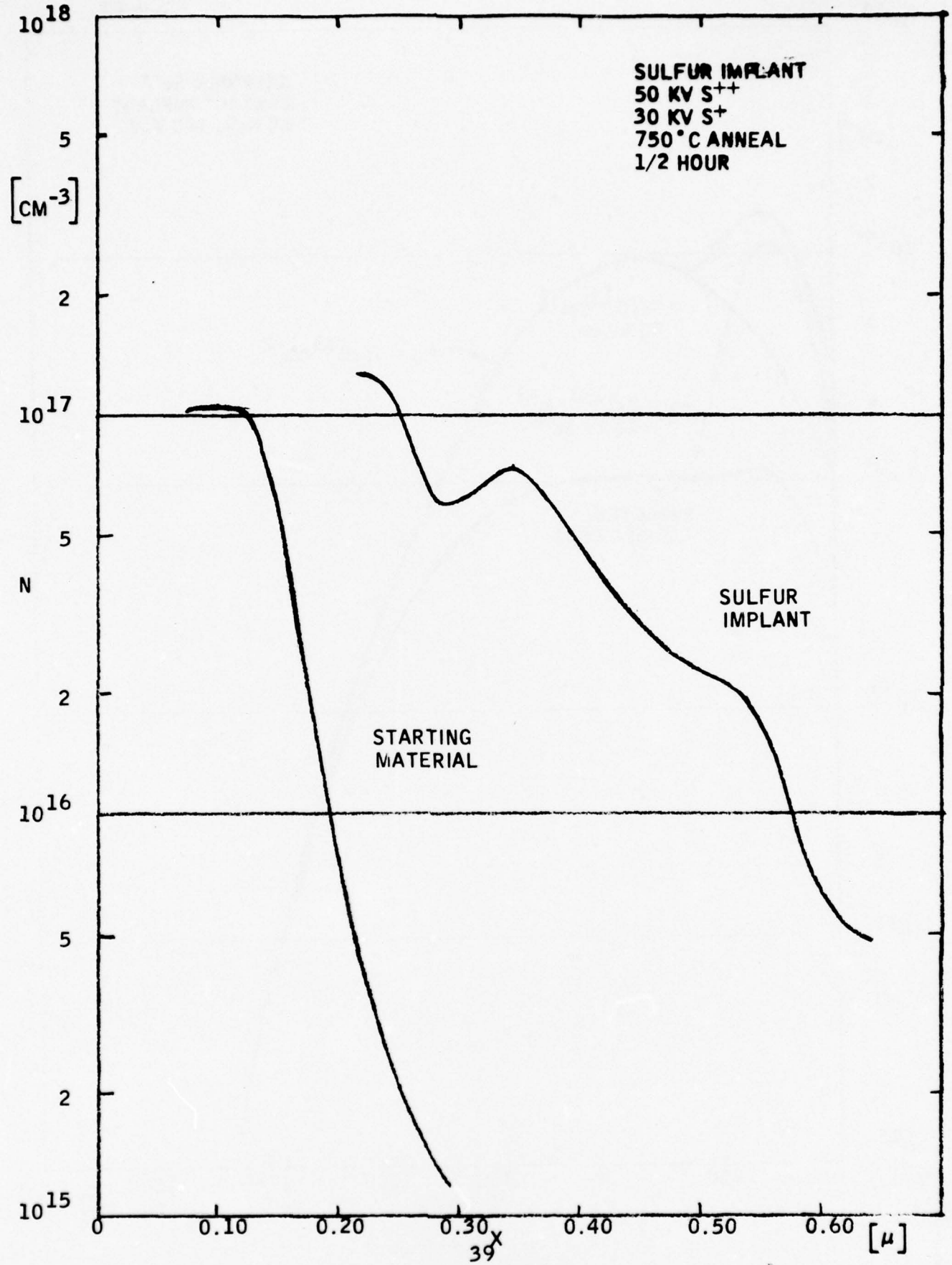
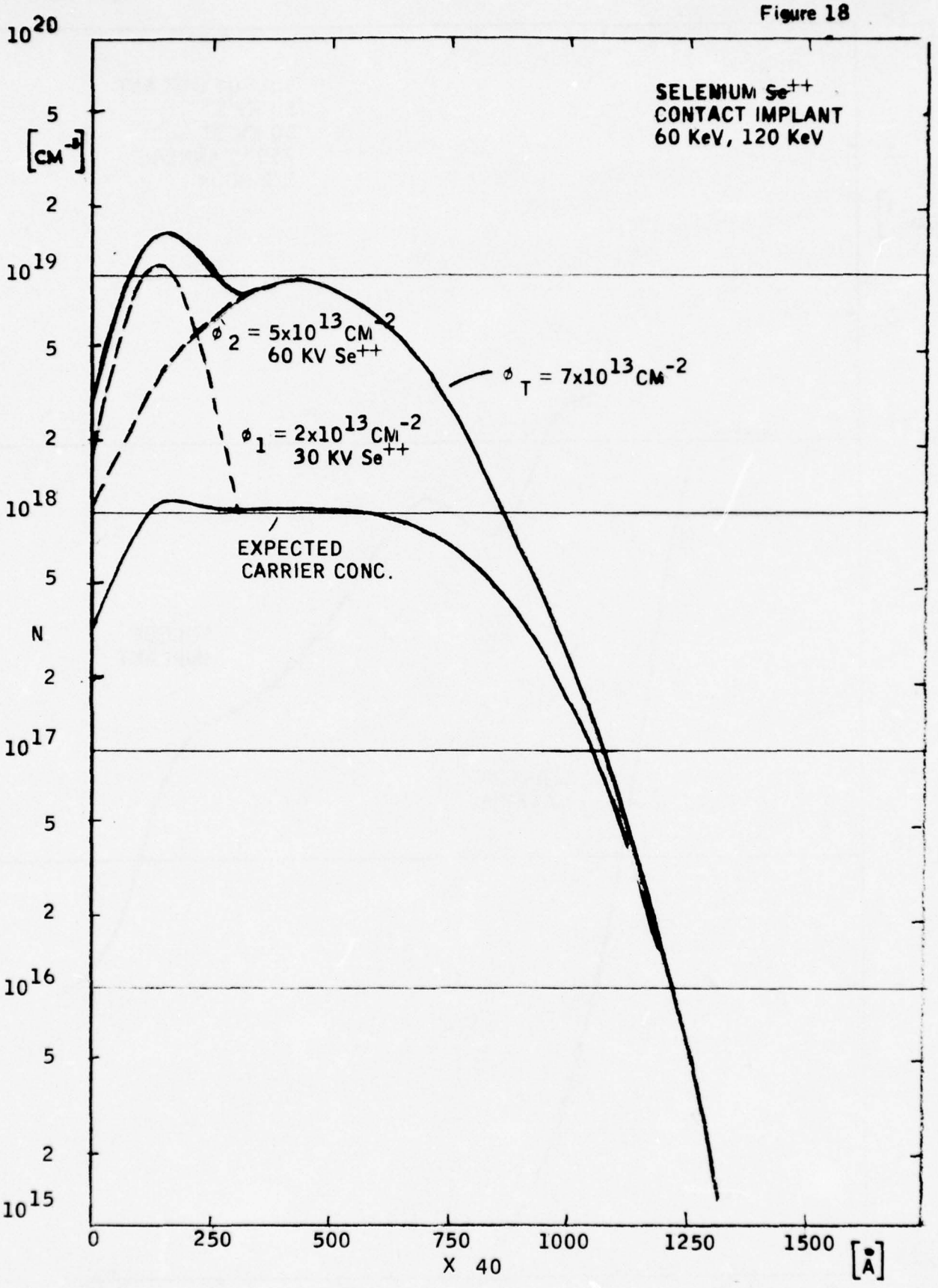

SULFUR IMPLANT
50 KV S++
30 KV S+
750°C ANNEAL
1/2 HOUR
SULFUR IMPLANT
STARTING MATERIAL
N
[CM-3]
10^18
5
2
10^17
5
2
10^16
5
2
10^15
0
0.10
0.20
0.30
0.40
0.50
0.60
[μ]

Figure 18


SELENIUM Se++
CONTACT IMPLANT
60 KeV, 120 KeV
$\phi_2 = 5\times10^{13}$ CM^{-2}
60 KV Se++
$\phi_T = 7\times10^{13}$ CM^{-2}
$\phi_1 = 2\times10^{13}$ CM^{-2}
30 KV Se++
EXPECTED
CARRIER CONC.
N
[CM^{-3}]
10^{20}
5
2
10^{19}
5
2
10^{18}
5
2
10^{17}
5
2
10^{16}
5
2
10^{15}
0
250
500
750
1000
1250
1500
X 40
[Å]

doses resulted in profiles which looked substantially the same as that of the starting material.

It is difficult to assess these results. However, it is suspected that oxygen is being implanted along with the sulfur, since oxygen and sulphur are difficult to separate by spectral analysis. Doubly charged sulfur, S++, with its atomic weight of 32 has a mass-to-charge ratio of 16; equal to that of singly charge oxygen, O+. In addition, singly charged sulfur is equal in mass/charge ratio to O_2^+. Singly charged sulfur occurs as H_2S^+ using hydrogen as the ionizing gas and should be distinguishable from O_2^+. Spectral analysis in our implanter, however, is accomplished using only 15° beam bending, and H_2S^+ could not be resolved.

In light of this problem, attention was directed toward the use of selenium as a contact dopant. From the point of view of depth of the implanted layer, Se is less attractive than sulfur. A 60 KV Se^+ implant, for instance, has a projected range, R_p, of 242 A° and a standard deviation of 121 A°, whereas a 60 KV, S^+ implant has a projected range of 446 A°, and standard deviation of 257 A°. This means that for a given charge, Qcm^{-2}, the peak doping of the Se^+ implant will be approximately twice that of the S^+ implant. As a result, the average mobility will be lower and hence the conductivity of the layer also lower. Nevertheless, Se was the only viable choice.

Solid selenium was used as the source for Se^{++} ions. Total dose, ϕ_T, was fixed at $7 \times 10^{13}/cm^2$, comprised of a 60 KV (120 Kev equivalent) implant with $\phi = 5 \times 10^{13}/cm^2$, and a 30 KV (60 Kev equivalent) implant with $\phi = 2 \times 10^{13}$. Figure 18 shows the LSS

curves and the predicted electron concentration taking doping degeneracy, doping efficiency and diffusion into account. Several wafers were implanted, using both buffer layer structures as well as Cr doped substrates. Substrate temperature was maintained at 400°C during the implant. A portion of the wafer was masked during implant to later allow the comparison of the implanted with unimplanted areas. Annealing was done using 1000 Å Si_3N_4 layer at 750°C for 1/2 hour. Figure 19 shows the impurity profile obtained by implanting Se^{++} ions into an epitaxial layer of 9×10^{15} cm^{-3} doping. Figure 20 shows the results obtained with the same implant schedule implanted into another epitaxial layer of $2 \times 10^{16} cm^{-3}$ doping.

Figure 21 shows the profile obtained with Se^{++} ions implanted into an N-type epitaxial layer which had been thinned to yield pinch-off voltage = 0 (i.e., the built-in voltage of the Schottky barrier, ~0.8 V, was sufficient to cause the depletion layer to reach the substrate).

(a) Contact Evaluation. Additional buffer layer samples were implanted with Se^{++} ions for the purpose of evaluating ohmic contacts made on these layers. Background doping was nominally $6 \times 10^{15} cm^{-3}$ for the buffer layer. Resulting profiles after implant and anneal are shown for three samples, 3K83, 84, and 86 in Figure 22. Approximately 1/2 of the wafer was masked against the implant to provide an area of control for the contact resistance comparison.

Figure 19

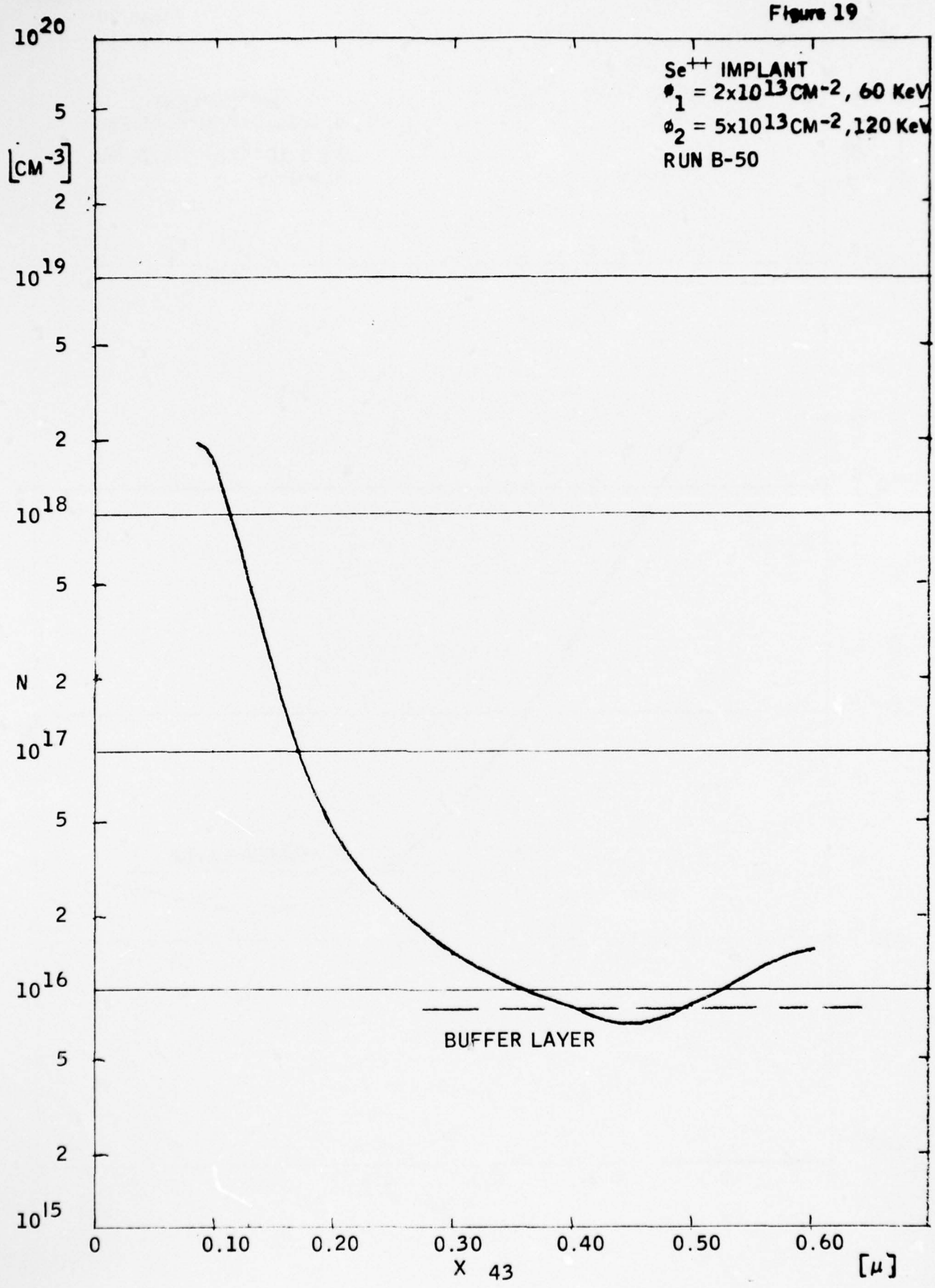

Se++ IMPLANT
ϕ_1 = 2x10^{13}CM^{-2}, 60 KeV
ϕ_2 = 5x10^{13}CM^{-2}, 120 KeV
RUN B-50
[CM^{-3}]
N
10^{20}
5
2
10^{19}
5
2
10^{18}
5
2
10^{17}
5
2
10^{16}
5
2
10^{15}
BUFFER LAYER
0
0.10
0.20
0.30
0.40
0.50
0.60
X 43
[μ]

Figure 28

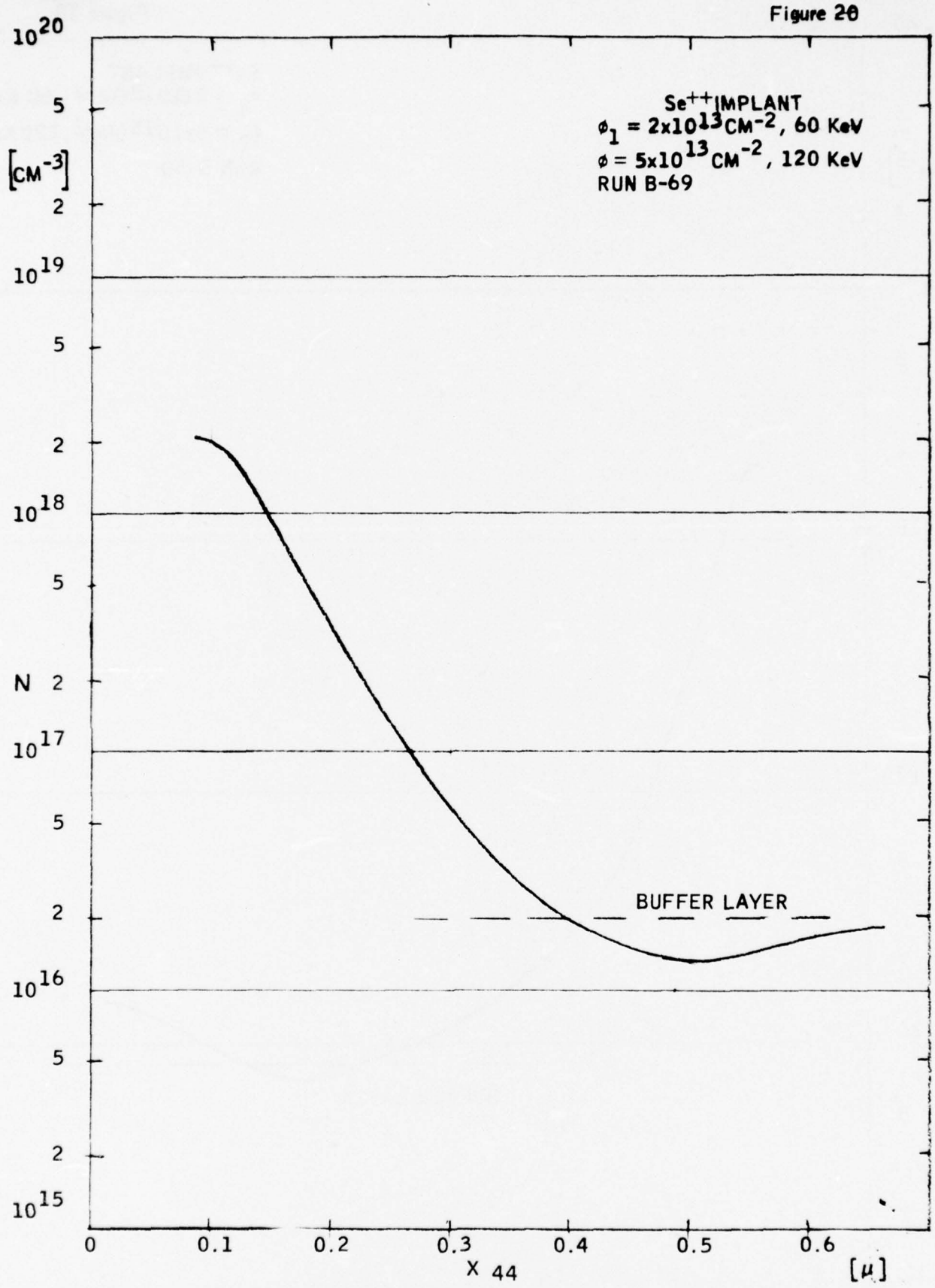

Se++ IMPLANT
$\phi_1 = 2 \times 10^{13} CM^{-2}$, 60 KeV
$\phi = 5 \times 10^{13} CM^{-2}$, 120 KeV
RUN B-69
BUFFER LAYER
N [CM^{-3}]
10^{20}
5
2
10^{19}
5
2
10^{18}
5
2
10^{17}
5
2
10^{16}
5
2
10^{15}
0
0.1
0.2
0.3
0.4
0.5
0.6
X 44
[μ]

Figure 21

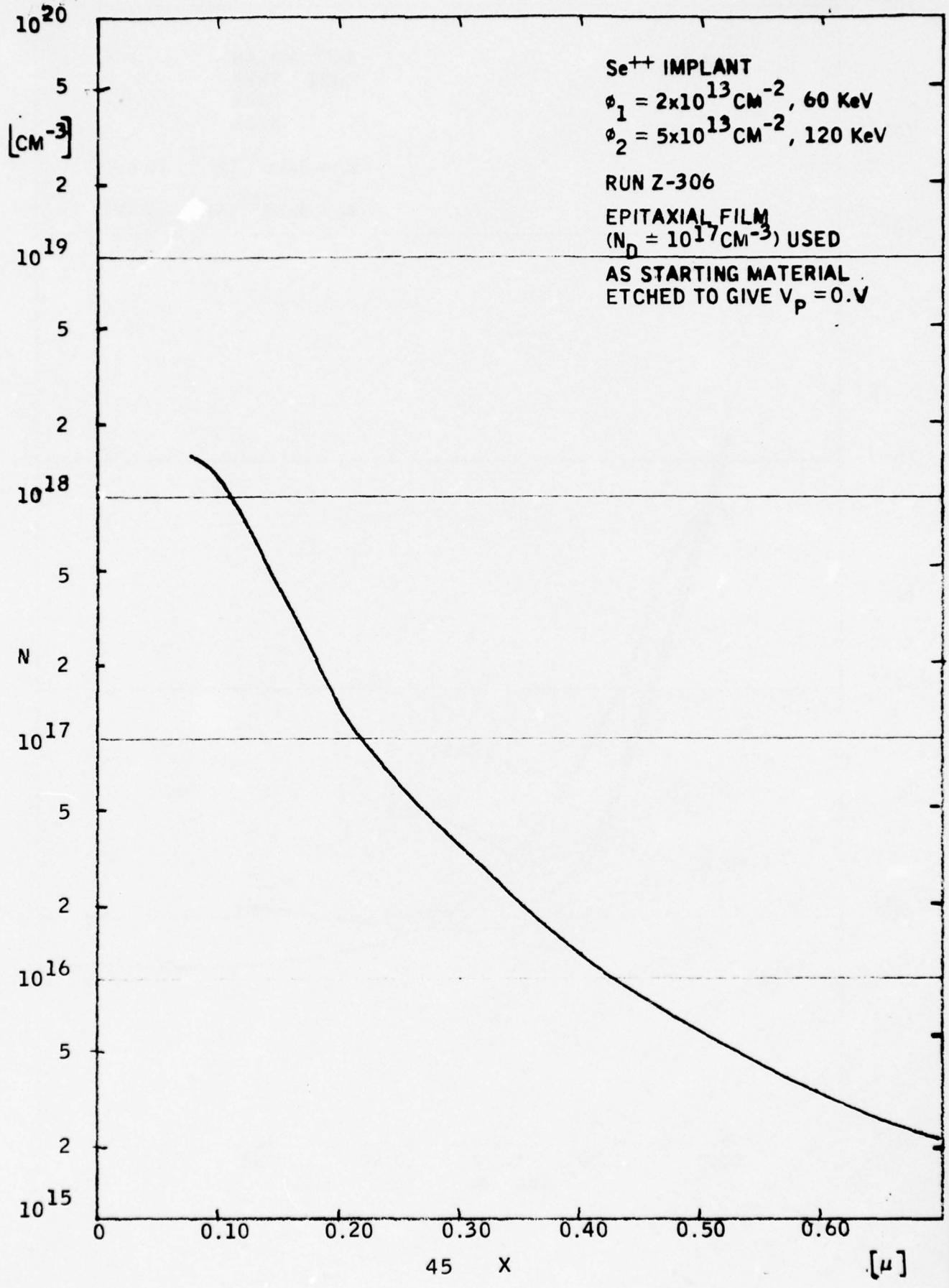
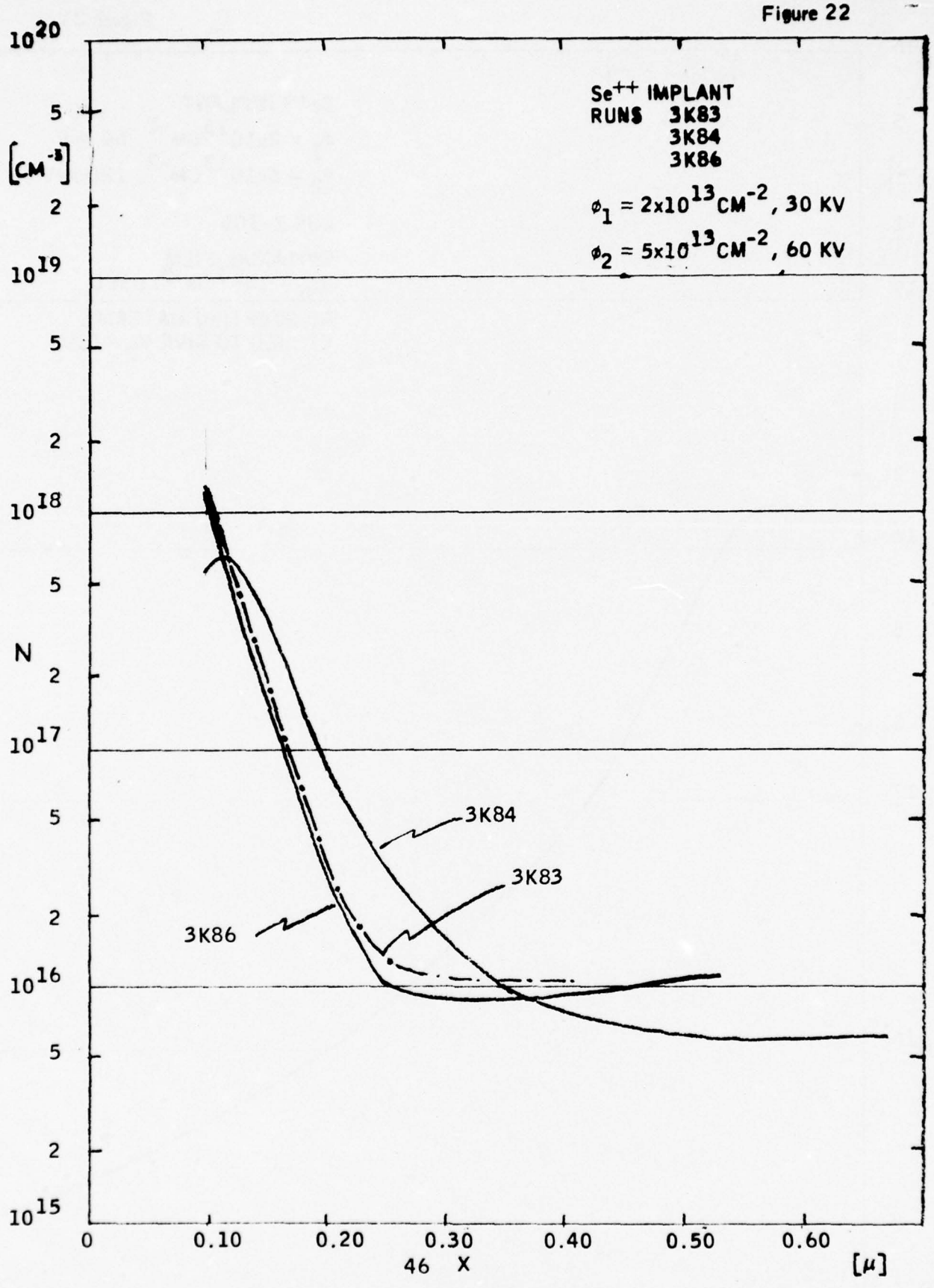

Se++ IMPLANT
$\phi_1 = 2 \times 10^{13} CM^{-2}$, 60 KeV
$\phi_2 = 5 \times 10^{13} CM^{-2}$, 120 KeV
RUN Z-306
EPITAXIAL FILM
($N_D \doteq 10^{17} CM^{-3}$) USED
AS STARTING MATERIAL
ETCHED TO GIVE $V_P = 0.V$
10^{20}
5
[CM^{-3}]
2
10^{19}
5
2
10^{18}
5
N
2
10^{17}
5
2
10^{16}
5
2
10^{15}
0
0.10
0.20
0.30
0.40
0.50
0.60
X
[μ]

Figure 22


Se++ IMPLANT
RUNS 3K83
3K84
3K86
$\phi_1 = 2 \times 10^{13} CM^{-2}$, 30 KV
$\phi_2 = 5 \times 10^{13} CM^{-2}$, 60 KV
10^{20}
5
$[CM^{-3}]$
2
10^{19}
5
2
10^{18}
5
N
2
10^{17}
5
2
10^{16}
5
2
10^{15}
3K84
3K83
3K86
0
0.10
0.20
0.30
0.40
0.50
0.60
[μ]
X

Contact resistance is determined using a special mask comprised of four contacts of different spacing. By measuring the resistance between each pair of contacts of different spacing both the sheet resistance, R_s, $\Omega/\square$, and the specific contact resistance, $\rho_c \Omega cm^2$, can be determined. Contact material is an alloy of Ge-Au, as for the GaAs FET. Surface preparation, metal evaporation and alloying also follow the FET fabrication schedule. Figure 23 shows the contact geometry used. The contacts are surrounded by an etched area to prevent current spreading around the contact edges. A plot of the resistance vs contact spacing is depicted in the figure. From the extrapolation of the data to $R_c = 0$ and the slope of the line defined by the data points, one can calculate the specific contact resistance, ρ_c, from $\rho_c = Rs\, L_T^2$.

Figure 24 shows typical resistance vs contact spacing for sample 3K83. It can be seen that although the sheet resistance in the implanted area is lower than that of the unimplanted area, the contact resistance is higher. Figure 25 shows SEM photos of the contact metal for sample 3K83 after alloy. Figure 25a shows the contact metal in the unimplanted area, while 25b shows the metal in the implanted area. The rough mottled appearance of the implanted side is typical of samples which show poor electrical behavior of the contacts.

Figure 23

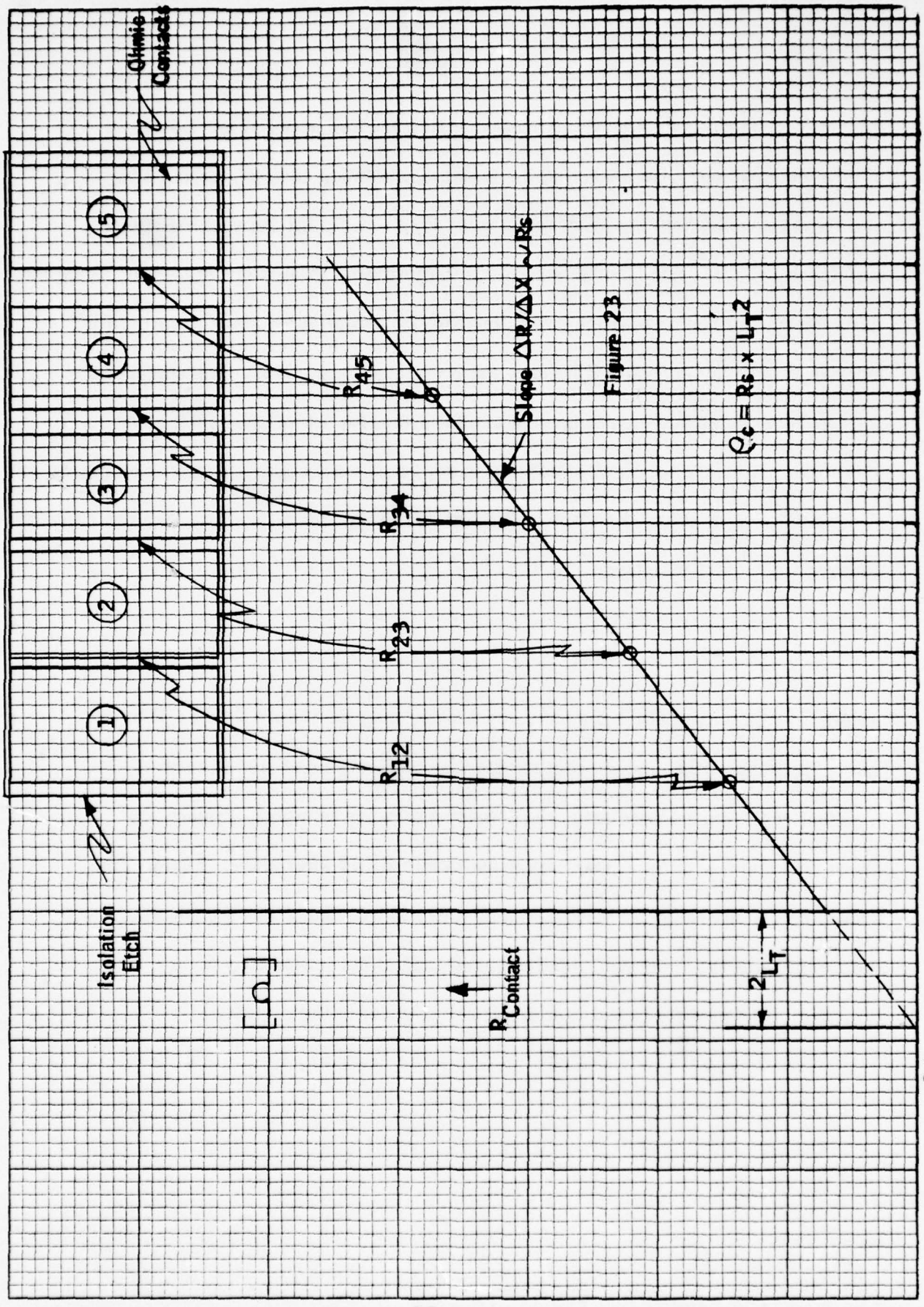
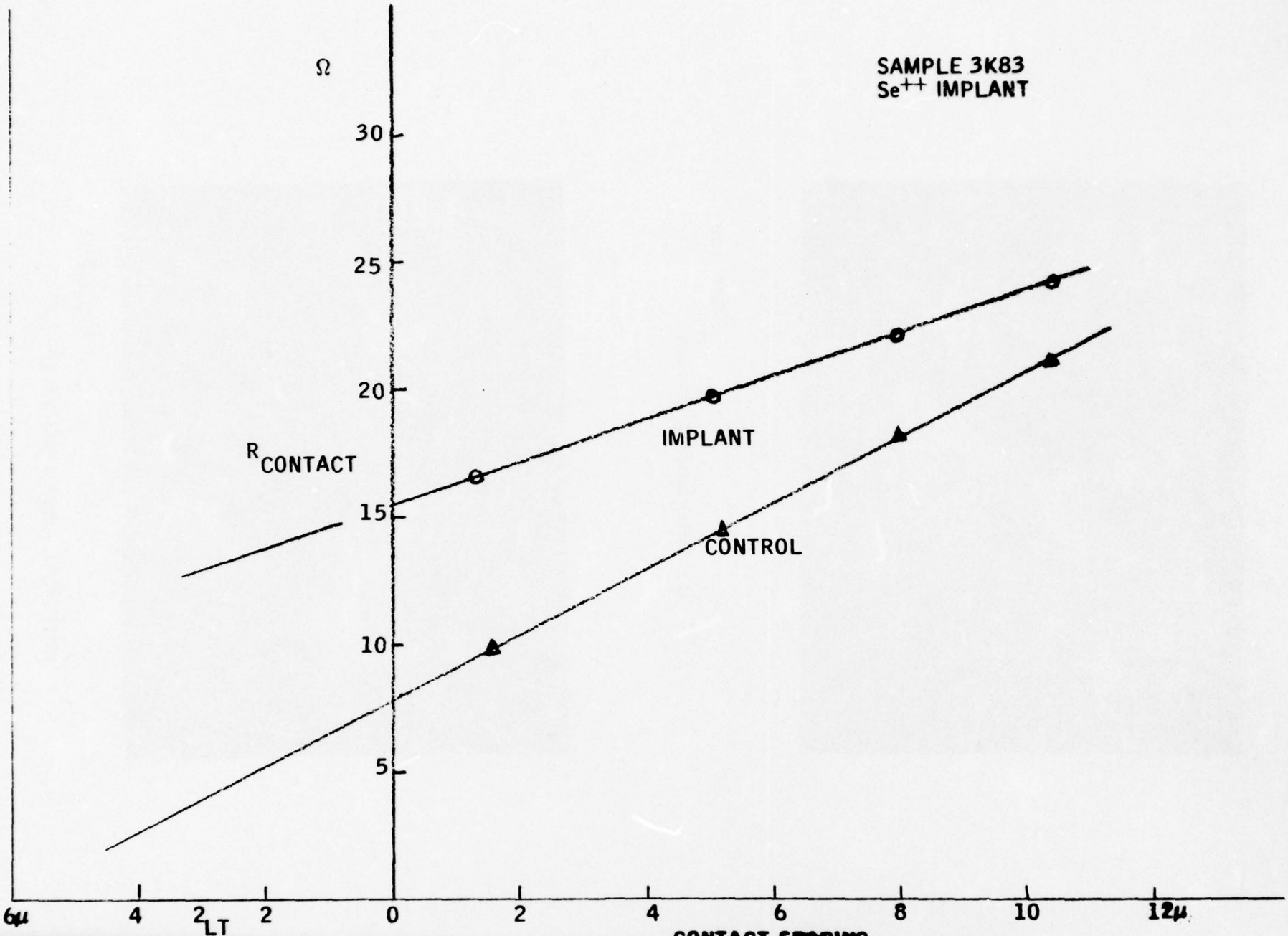

Ohmic Contacts
Isolation Etch
1
2
3
4
5
R_{12}
R_{23}
R_{34}
R_{45}
Slope $\Delta R/\Delta X = R_S$
$\rho_c = R_S \times L_T^2$
$R_{Contact}$
$2L_T$
$2L_T$
X
Contact Spacing
[Microns]
[Ω]

Figure 24



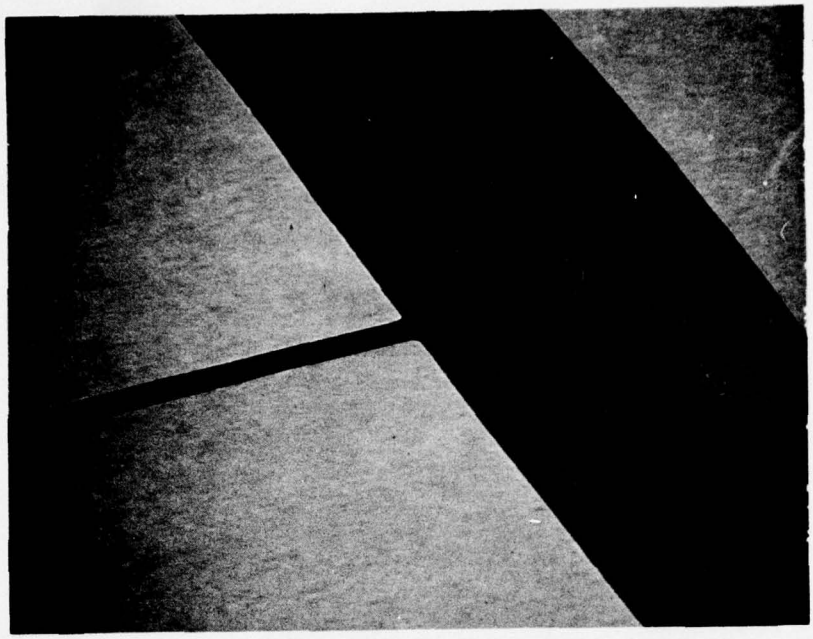


Figure 25a

Typical Metal Unimplanted Area

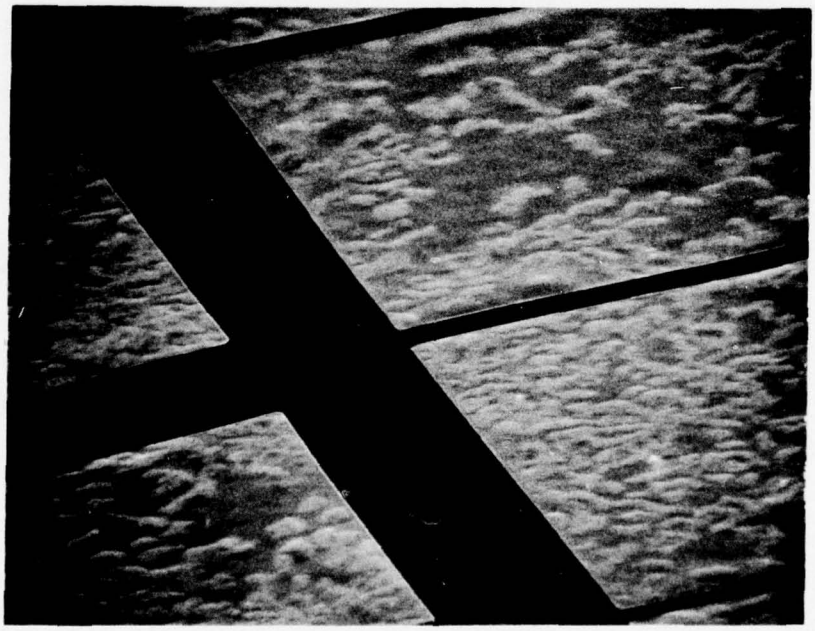


Figure 25b

Typical Metal Appearance Implanted Area

Figure 26

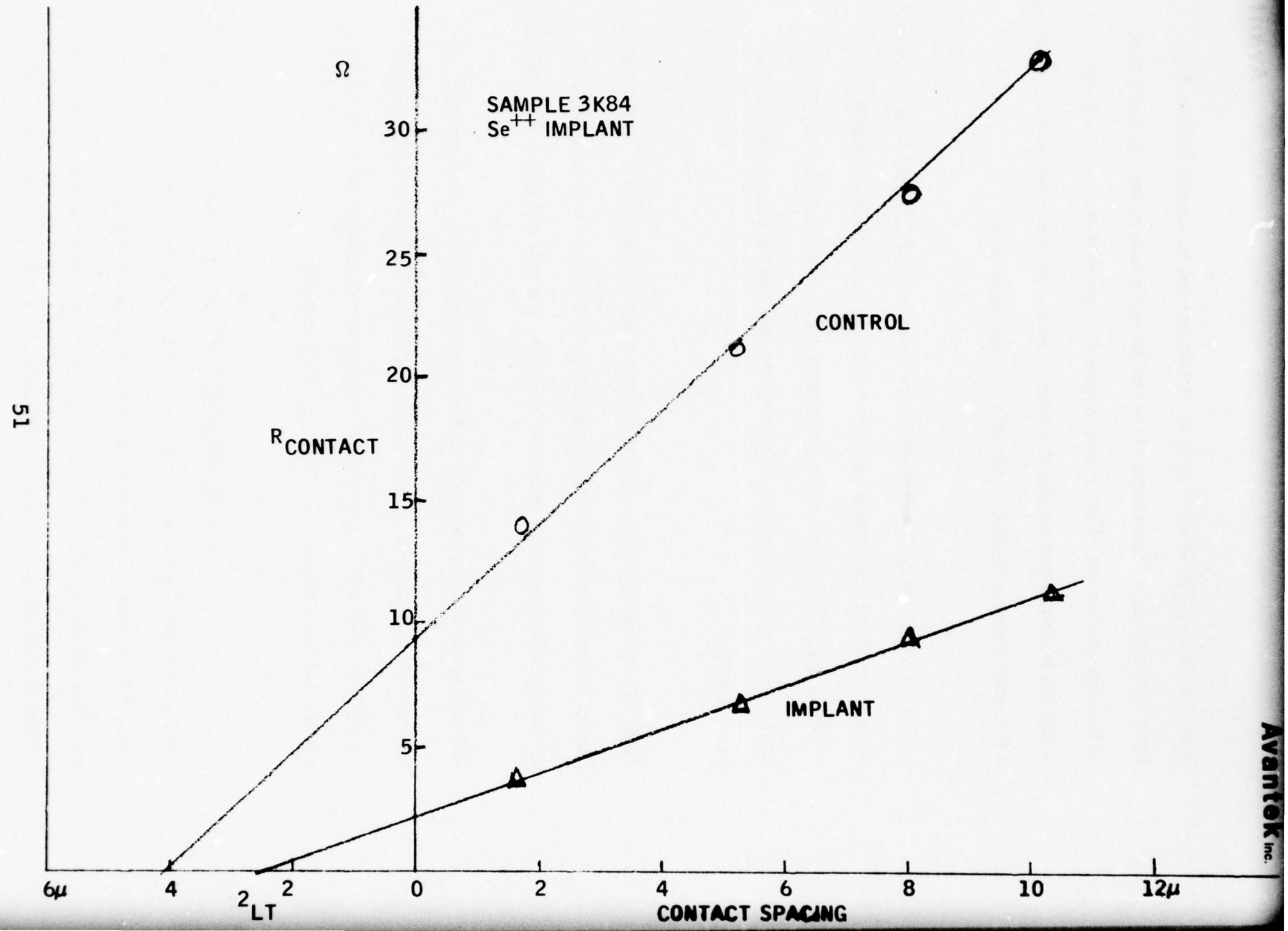


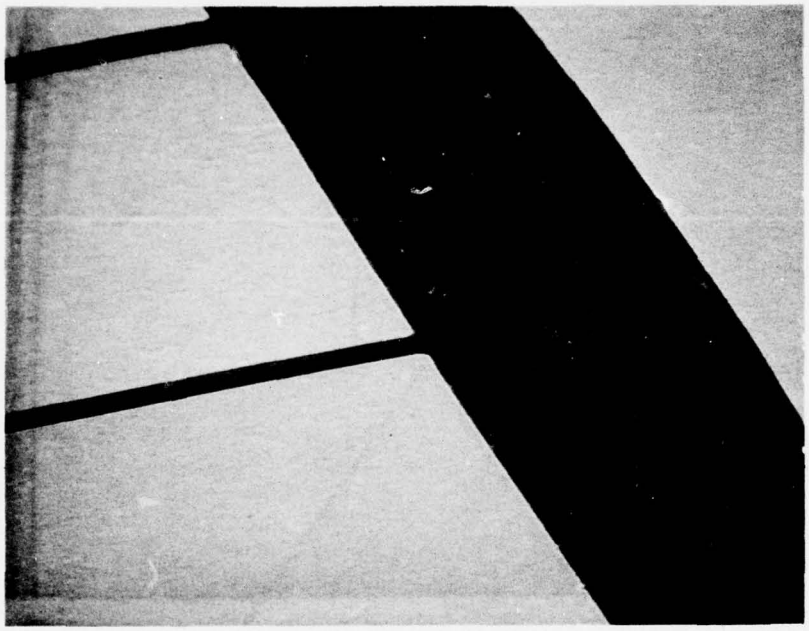
Figure 26 shows typical resistance vs contact spacing for sample 3K84. Here there is a noticeable improvement in the contact resistance as well as a reduction in the sheet resistance. Furthermore, Figure 27, an SEM photo of the contacts, shows the implanted and unimplanted areas to have identically the same appearance, a fine grain structure typical of contacts with low resistance.

Figure 28 shows typical contact resistance data for sample 3K86. The appearance of the contacts for this sample were very similar to those of sample 3K84, shown in Figure 27. There is considerable variation in the electrical behavior of all three of these contact samples, in spite of the fact that the processing steps were kept identical.

Table III is a summary of ion implanted layers processed during this report period. Contact resistance and sheet resistance data, where shown, were obtained using the contact resistance mask shown in Figure 23, and data of Figures 24, 26, & 28.

Although some encouraging results with contact implants have been achieved, the odds have been in favor of poorer contact quality with implantation than without. Furthermore, what may be construed as some degree of success has been achieved with the contact resistance test mask, not FET contacts.

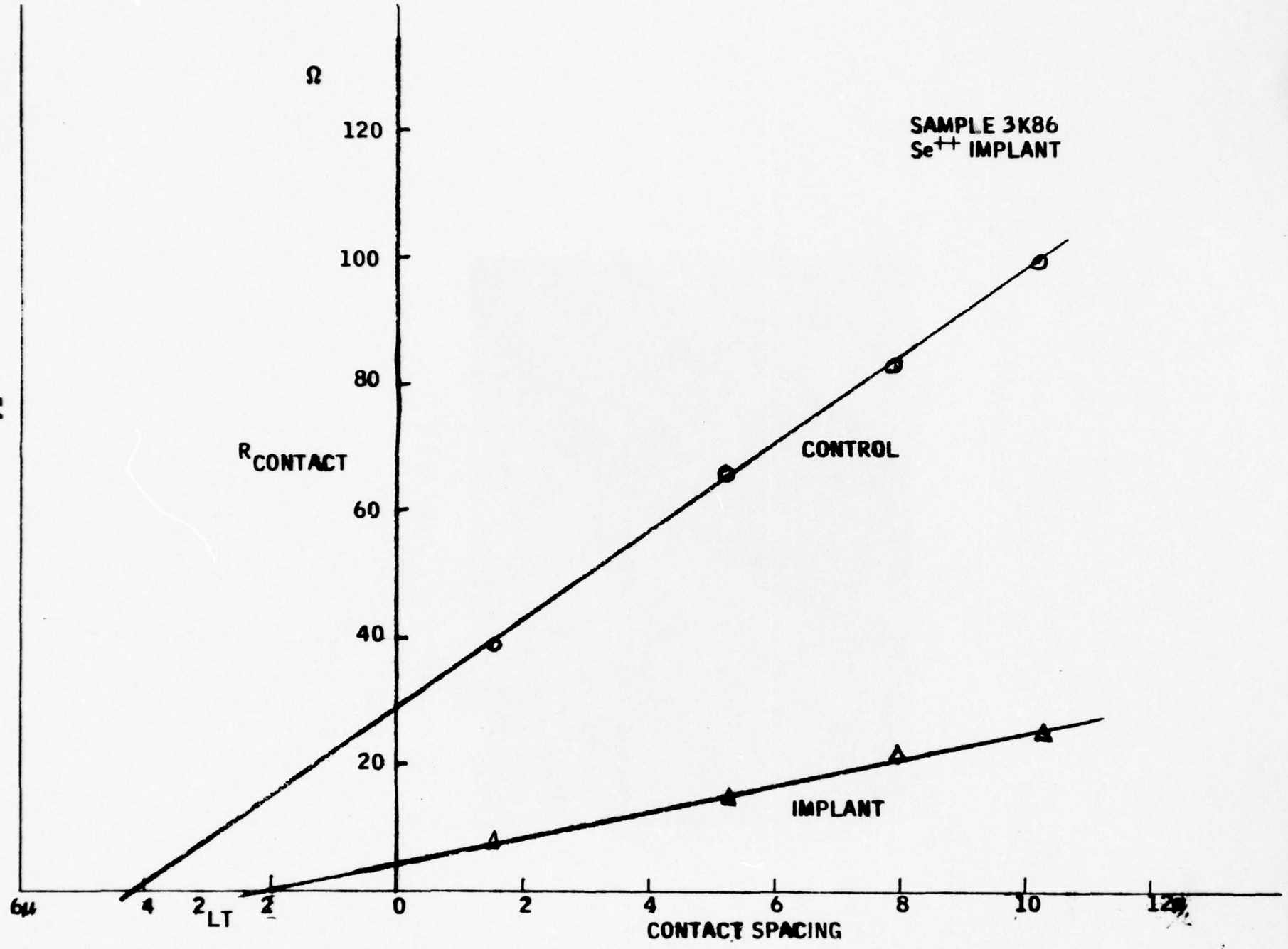
(iii) Ion Implanted FET Contacts. The contact implantation process using Se^{++} which has shown some encouraging results was extended to GaAs FET contacts. The process is somewhat different in that all of the test data from Table III was obtained by evaluating a uniformly implanted layer. In this way not only is contact resistance determined, but also the sheet resistance of the



SEM Photo, Contact 3K84

Figure 27

Figure 28



Run	Substrates	Q/cm^2 Implanted Se^{++}	R_s Buffer Layer $\Omega/\square$	R_s Buffer Plus Implant	ρ_c Buffer Ωcm^2	ρ_c Implant Ωcm^2
3K-7	Buffer Layer $N_D = 6 \times 10^{16}$	8×10^{13} Double Implant	105	80	1×10^{-5}	2.9×10^{-6}
P-698	Cr Doped	"	--	200	--	1.2×10^{-6}
B-50	Buffer $N_D = 1 \times 10^{16}$	7×10^{13} "	1000	230	4×10^{-5}	5×10^{-6}
B-69	"	5×10^{13} Single Implant	2000	550	1×10^{-4}	3×10^{-6}
Y-1322	" $N_D = 1 \times 10^{17}$	7×10^{13} Double Implant	900	600	6×10^{-6}	10^{-5}
Z-306	"	"	Thinned To Give $V_p = 0$	475	--	2×10^{-5}
3K-83	" $N_D = 2 \times 10^{16}$	"	350	200	$>10^{-3}$	$>10^{-3}$
3K-84	"	"	575	200	2×10^{-5}	2×10^{-6}
3K-86	" $N_D = 10^{16}$	"	1700	500	1×10^{-4}	7×10^{-6}

TABLE III

Summary of Se^{++} Contact Implants

implanted layer. In the case of an FET, however, the implanted areas must be confined to the contact area. This can be accomplished by either selectively implanting into the contact areas or implanting the entire surface, and selectively removing the implanted portion outside the contacts. Selective implant in the contact areas was chosen.

A layer of Si_3N_4 was deposited over the entire surface of an N-type GaAs wafer which had been selected for FET fabrication. The Si_3N_4 layer was chosen to be sufficiently thick that it would mask against 120 Kev Se. Contact areas were etched open, and these areas implanted with a total dose of $7 \times 10^{13} cm^{-2}$ of Se^{++} ions, with the substrate at ~400°C. Samples were masked off during implantation to provide an area on the wafer as a control. The sample was then coated with 1000Å of Si_3N_4, and annealed at 750°C for 1/2 hour. The Si_3N_4 was etched out of the contact areas and the sample masked for contact metal evaporation.

From this point all processing followed standard FET fabrication procedures. Evaluation of samples prepared in this way in all cases give disappointing results. Contacts in the implanted areas were inferior to those in the unimplanted areas. The surface of the metal was typically rough and blistered in appearance, similar to that shown in Figure 29b. In addition, the contacts in the unimplanted areas were found to be substantially inferior to those produced on wafers in the same run which had been held out of the implantation process entirely, i.e., no high

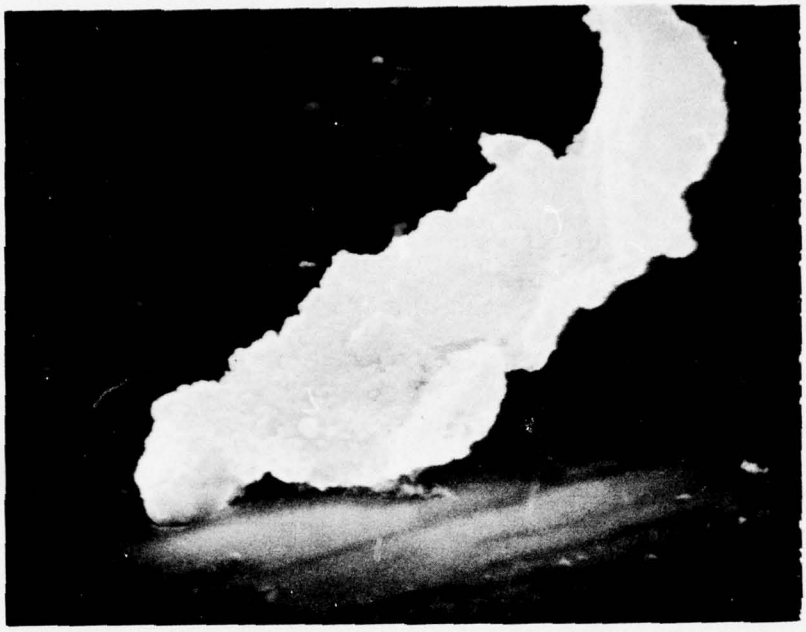
temperature annealing.

These results indicated the possibility of problems with the Si_3N_4 cap used to anneal the ion implant. At this time therefore, a concentrated effort was placed on a thorough evaluation of the Si_3N_4 film.

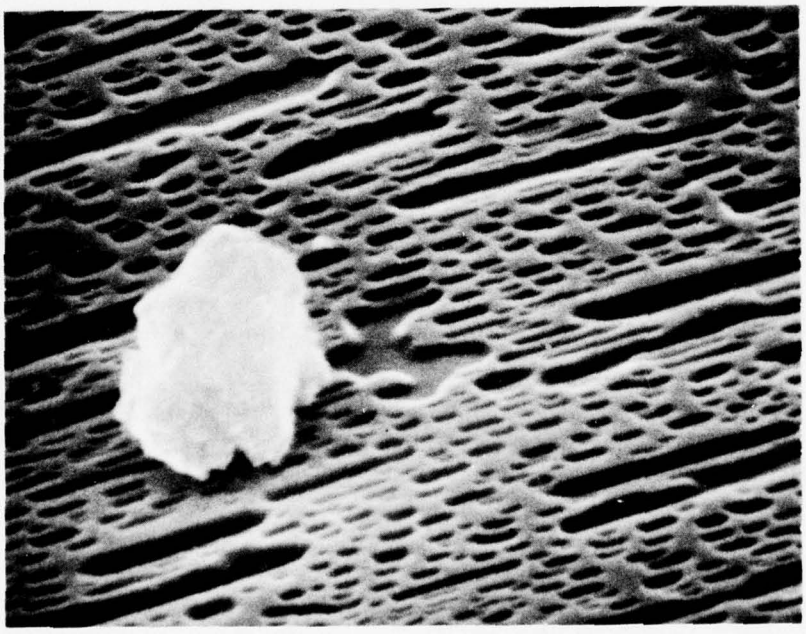
(a) Evaluation of Si_3N_4 Annealing Cap. Si_3N_4 deposited in a variety of ways, is commonly used as an annealing cap for GaAs ion implants. In addition, SiO_2 and AlN are also used. The disadvantage of SiO_2 is that it does not mask against Ga out-diffusion which occurs during the annealing step. AlN, although forming a good mask to diffusion of impurities, is difficult to remove.

During the course of the deposition and annealing experiments with Si_3N_4 layers, large variations were found in both the index of refraction and film thickness for precisely controlled power and gas flow settings. In particular, the index could not be well predicted from run to run. Values of 1.85 - 2.3 were obtained randomly for the same power and gas flow settings. In addition, following the 750°C annealing step, the surface of the GaAs quite frequently showed eroded areas and pits. In some cases, the Si_3N_4 film showed flaking or blistering after the annealing step.

Figure 29 shows an SEM photograph of an GaAs wafer which had been coated with 1000Å of Si_3N_4, and annealed at 750°C for 1/2 hour. Prior to the annealing step,



GaAs Surface Prior to Silicon Nitride Removal
Figure 29a

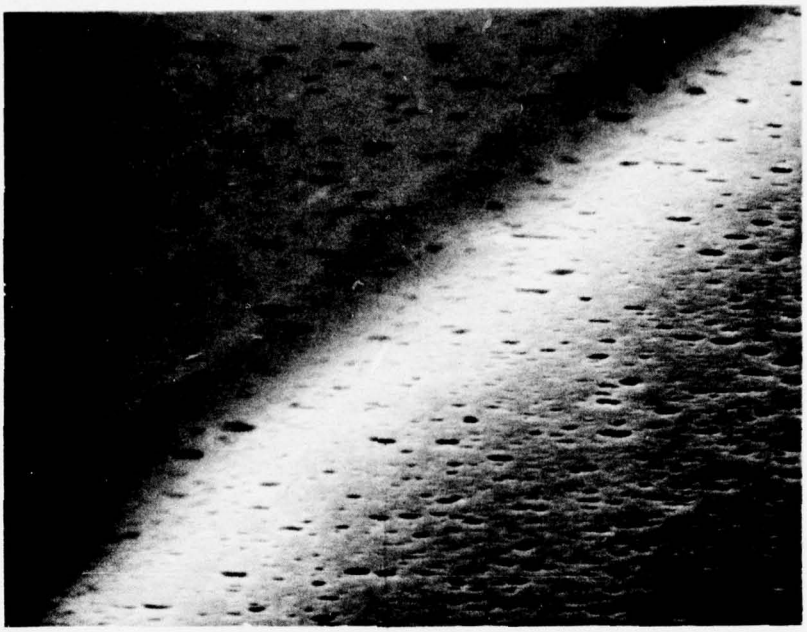


GaAs Surface After Silicon Nitride Removal
Figure 29b

the surface of the GaAs and the Si_3N_4 were smooth and featureless.

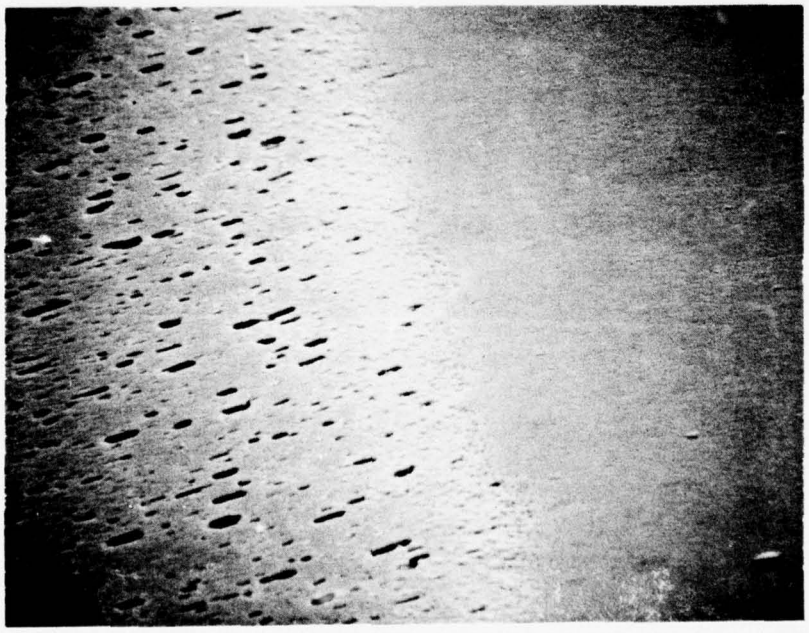
Figure 29a shows the sample prior to removal of the Si_3N_4 film. Small spots on the surface of the Si_3N_4 film can be seen, which appear to be associated with dark areas under the film. In many areas very large eruptions appear through obvious defects in the film. In other areas, the dark regions under the film do not appear to be associated with defects in the integrity of the film. Figure 29b shows the appearance of the GaAs surface after removal of the Si_3N_4. An electron microprobe analysis of the surface eruptions shows them to be Ga rich.

Figure 30a shows an SEM photo of another GaAs sample coated with 1000Å Si_3N_4, and annealed at 750°C for 1/2 hour. A portion of the film was removed as indicated in the photo. This area is seen to the right of the white boundary line. Surface pits are evident in the area under the Si_3N_4 film as well as in the etched portion. There appear to be no defects in the surface of the film which might have caused the formation of the pits. In order to verify this, the sample was coated with ~200Å of Au and re-examined in the SEM. Figure 30b shows the area in which the Au was evaporated over the Si_3N_4 to be free of pits. (This area is now seen in the right hand portion of the photo) The pits, therefore, do not appear to develop as a result of mechanical defects (such as holes) in the Si_3N_4 film. They may be due to loss of Ga into an oxide rich film. Also, interfaced defects (small voids) could be generated as the Si_3N_4 films are first laid down.



SEM, GaAs, 1000Å, Si_3N_4, 750° Anneal

Figure 30a



SEM, GaAs, 1000Å, Si_3N_4, 750° Anneal
(Includes Area Protected by Gold)

Figure 30b

Adjustments in the reactor phasing produced Si_3N_4 films which show N= 2.0 to 2.03 over a wide range of RF power. Si_3N_4 films deposited after this improvement in the reactor permit annealing of GaAs wafers at temperatures as high as 900°C for 1 hour with no surface degradation after removal of the Si_3N_4 film.

b. Active Layer Implants: In light of the disappointing results thus far obtained with FET contact implantation, a decision was made to redirect effort to lighter dose implants using Se^{++} in an attempt to fabricate films suitable for the active layer of the GaAs FET.

(i) Implantation into Cr Doped Substrates.

(a) Substrate Qualification. Implantation into Cr doped substrates without buffer layers imposes special requirements on the quality of the substrate with regard to surface conversion at annealing temperatures in excess of 800°C. It has been frequently found that Cr doped substrates which are semi-insulating prior to exposure at high temperatures become heavily conductive after annealing for a relatively short period of time at 800-900°C. We have found that a 900°C, 15 minute anneal in many cases causes a semi-insulating substrate to exhibit n-type behavior with $N_D \approx 10^{17}$ cm^{-3}, and mobility of 2000 $\sim cm^2V^{-1}$ sec^{-1}. This n-type film extends several microns into the substrate after annealing. Implantation into such a substrate would, after annealing, exhibit the implanted impurity distribution plus a 10^{17} cm^{-3} plateau

due to the surface conversion. Fabrication of ion implanted FETs would be impossible using such a substrate. We therefore undertook a program to "qualify" substrates for use in ion implantation, utilizing the surface breakdown voltage of the substrate, measured before and after the annealing process, the qualifying criterion.

Substrates are cleaned very carefully and etched, using the same procedure as that for epi growth preparation. Surface breakdown voltage is measured using a pair of blunt gold probes of approximately 5 mm spacing. Breakdown voltage is measured on a Tektronix curve tracer with 1500 V sweep capability. In all cases, before annealing, V_B is >1,000V, and generally 1,400V.

Substrates are then cleaned (but not etched) and coated with 1000Å of Si_3N_4, which is annealed at 900°C for 1/2 hour. The Si_3N_4 is then stripped, and the surface breakdown remeasured. Substrates which have converted will typically show $V_B \cong 20V$, whereas those which do not convert (i.e., "qualify") will show V_B >1000V. In most cases, those wafers which qualify will have breakdown voltages equal to or better than the pre-anneal values. Table IV shows the qualification test results of substrates from Suppliers A, B, and C. Breakdown voltage before and after 900°C anneal are shown.

The qualification of buffer layers is somewhat different. In this case, where the doping concentration is measurable, the buffer layer sample is profiled before and after the

Supplier	V_B Surface Before Anneal	V_B Surface After Anneal
A	1200V	1000-1400V
A	1400V	1400V
A	1000V	12V *
A	1200V	300V *
A	1400V	1200V
A	1300V	1400V
A	1200V	1200V
A	1200V	20V *
B	1200V	15V *
B	1400V	10V *
B	1400V	10V *
B	1200V	15V *
C	1000V	20V *

*REJECTED

TABLE IV

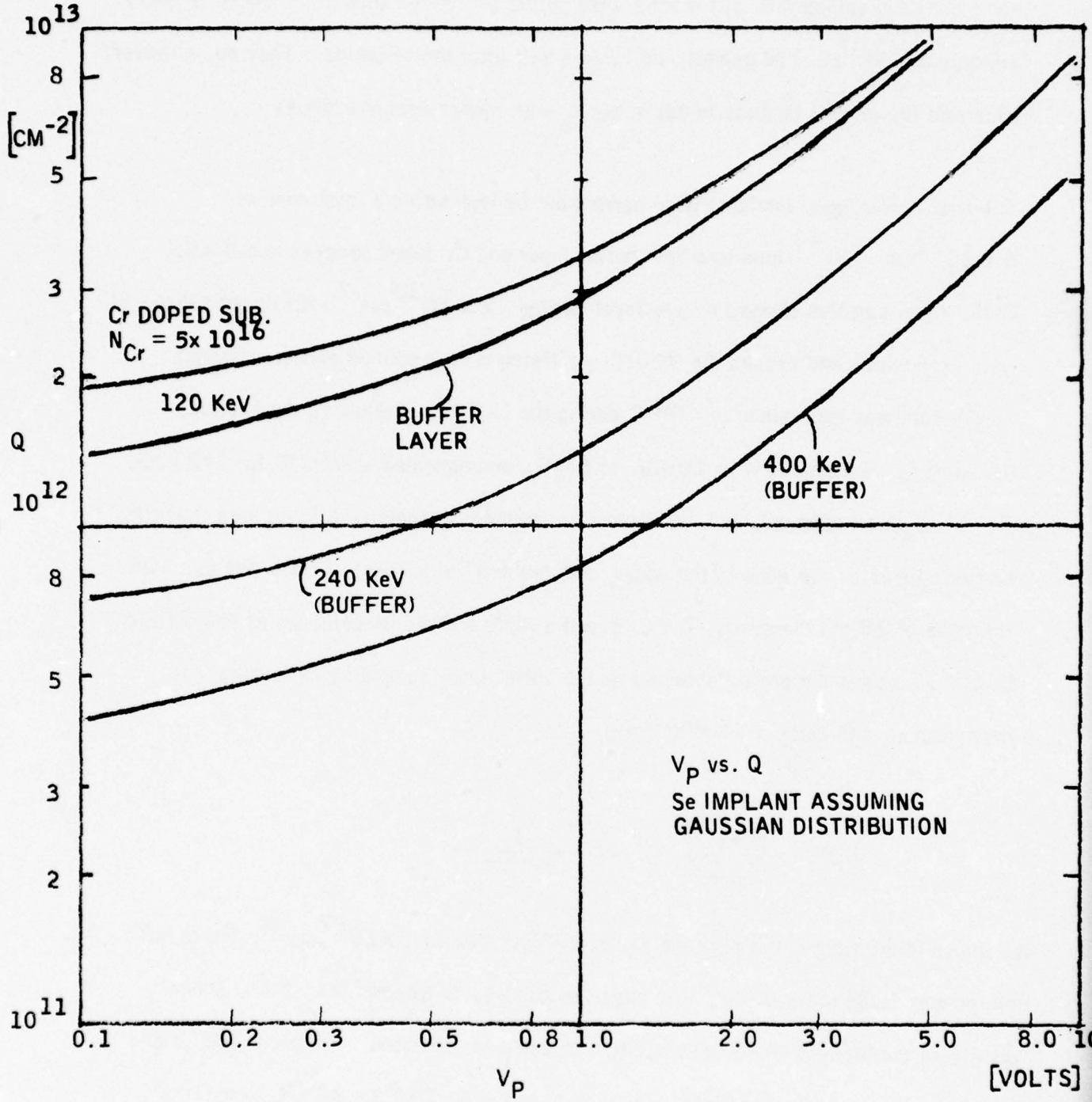
Surface Breakdown Voltage of Cr Doped Substrate Samples Before and After 900°C Anneal. Samples are from three suppliers.

Si_3N_4 deposition and annealing process. Any changes in the doping concentration which occur due to the temperature cycle can be detected in this manner. Either Cr doped or buffer layer substrates which do not satisfy minimum requirements with respect to breakdown voltage degradation or doping level are rejected.

(b) Implantation. Using Se^{++} ions implanted at 60 KV (120 Kev), the required dose for an active layer is estimated as follows: Assuming as a first approximation (which is an oversimplification) that the electrically active impurity distribution is Gaussian, curves of N(X) vs X are plotted for different charges, Q cm^{-2}. The voltage required to displace this charge (i.e., pinch off the film) was calculated for each dose. Figure 31 shows pinch off voltage vs Q cm^{-2}, with equivalent energy, Kev, as the parameter. Although Avantek's capability is indicated at 120 Kev, curves for 240 Kev and 400 Kev are shown for interest. The curves include the built-in voltage of ~ 0.8V in the pinch off voltage. Curves are shown for both buffer layers and Cr doped substrates in which $N_{cr} = 5X10^{16}$. Q cm^{-2} vs V_p in Figure 29 pertains to 100% electrical activity. The actual pinch-off would be determined by taking into account the actual activity of <100%.

Of interest to note on the 120 Kev curves is that a charge of $5X10^{12}$ cm^{-2} will be depleted with ~2.5 V (~2.0V on a Cr doped substrate). However, if one assumes that avalanche occurs in GaAs when the electric field reaches ~$5X10^5$ v/cm, then $5X10^{12}$ charges cm^{-2} is about as far as one can go. With a 400 Kev implant, however, the

Figure 31


10^{13}
8
[CM^{-2}]
5
3
2
Q
10^{12}
8
5
3
2
10^{11}
Cr DOPED SUB.
$N_{Cr} = 5 \times 10^{16}$
120 KeV
BUFFER LAYER
400 KeV (BUFFER)
240 KeV (BUFFER)
V_P vs. Q
Se IMPLANT ASSUMING GAUSSIAN DISTRIBUTION
0.1
0.2
0.3
0.5
0.8
1.0
2.0
3.0
5.0
8.0
10
V_P
[VOLTS]

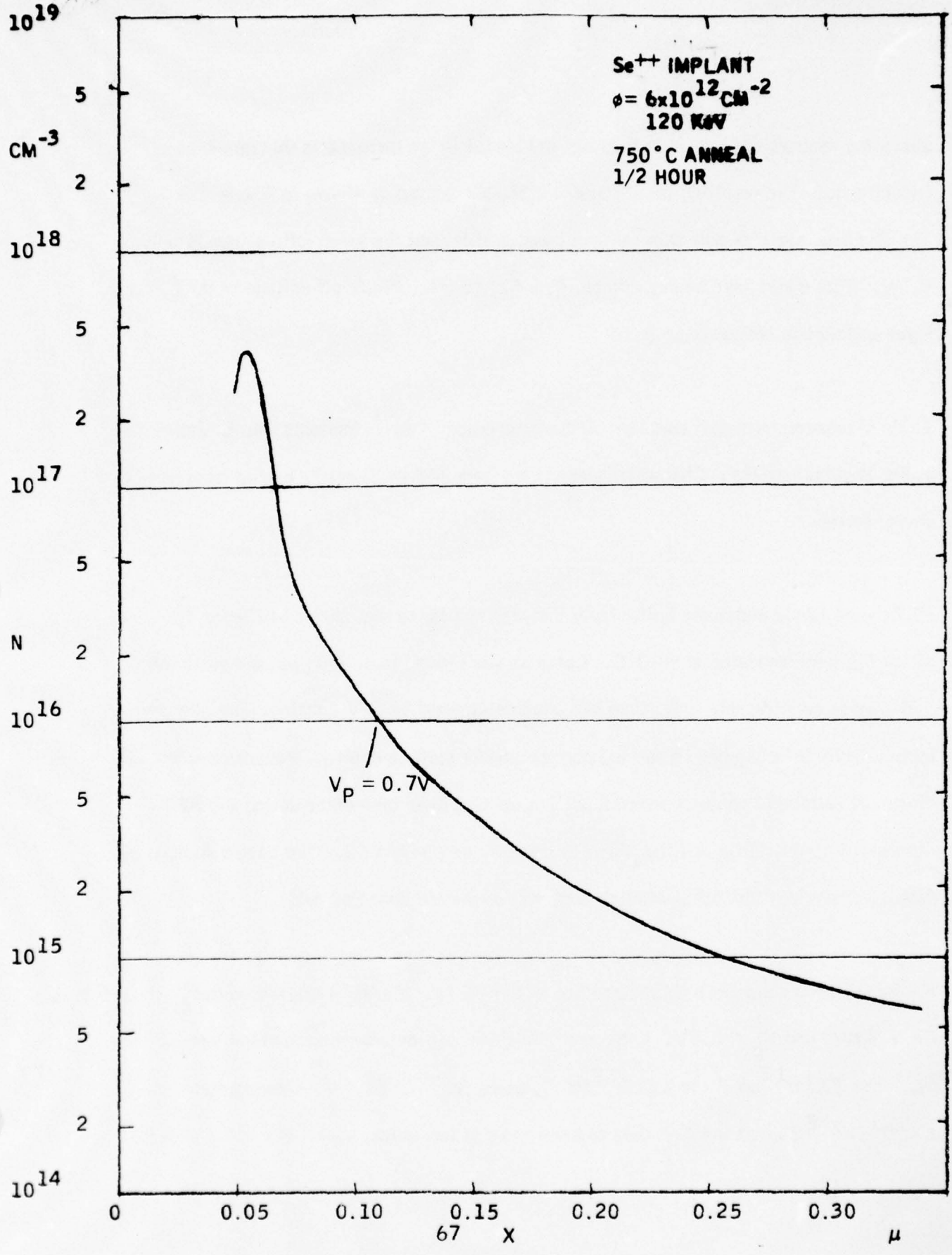
same charge displacement will require 10V before avalanche sets in. These numbers are only a guideline, and geometrical factors will alter the situation. They do, however, illustrate the greater latitude in adjusting V_p with higher energy implants.

The first active layer implants were carried out by implanting a total dose of $6 \times 10^{12} cm^{-2}$ Se^{++} ions into both buffer layer and Cr doped samples at 60 KV. Buffer layer samples showed n-type layer doping $7 \times 10^{13} cm^{-2}$. Cr doped substrates were used which had passed the 900°C qualifying test described earlier. Sample temperature was maintained at 400°C during the implant. Following the implant, the samples were coated with 1000Å of Si_3N_4 and annealed at 750°C for 1/2 hour. The Si_3N_4 was removed, and the implants evaluated by applying a large area Schottky barrier contact at one edge of the wafer, and probing the balance of the wafer using an Hg probe of 20 mil diameter. The Cr doped sample showed no evidence of implantation. Figure 32 shows the profile obtained on the buffer layer sample by measuring capacitance, and calculating N(X) from:

$$N(X) = \frac{[C(X)]^3}{qKA^2} \cdot \frac{1}{-dc/dV}$$

As shown in the figure, the peak doping is approximately $3.5X10^{17} cm^{-3}$. Pinch-off voltage was found to be 0.7V. The question arose as to whether the 750°C anneal was giving the highest electrical activity that could be expected. Additional buffer and Cr doped samples implanted identically were annealed at 750°C, 825°C, and 900°C for 1/2 hour. A substantial increase in the electrical activity was observed as the

Figure 32


Se++ IMPLANT
φ= 6x10^12 CM^-2
120 KeV
750°C ANNEAL
1/2 HOUR
10^19
5
CM^-3
2
10^18
5
2
10^17
5
N
2
10^16
5
2
10^15
5
2
10^14
V_P = 0.7V
0
0.05
0.10
0.15
0.20
0.25
0.30
X
μ

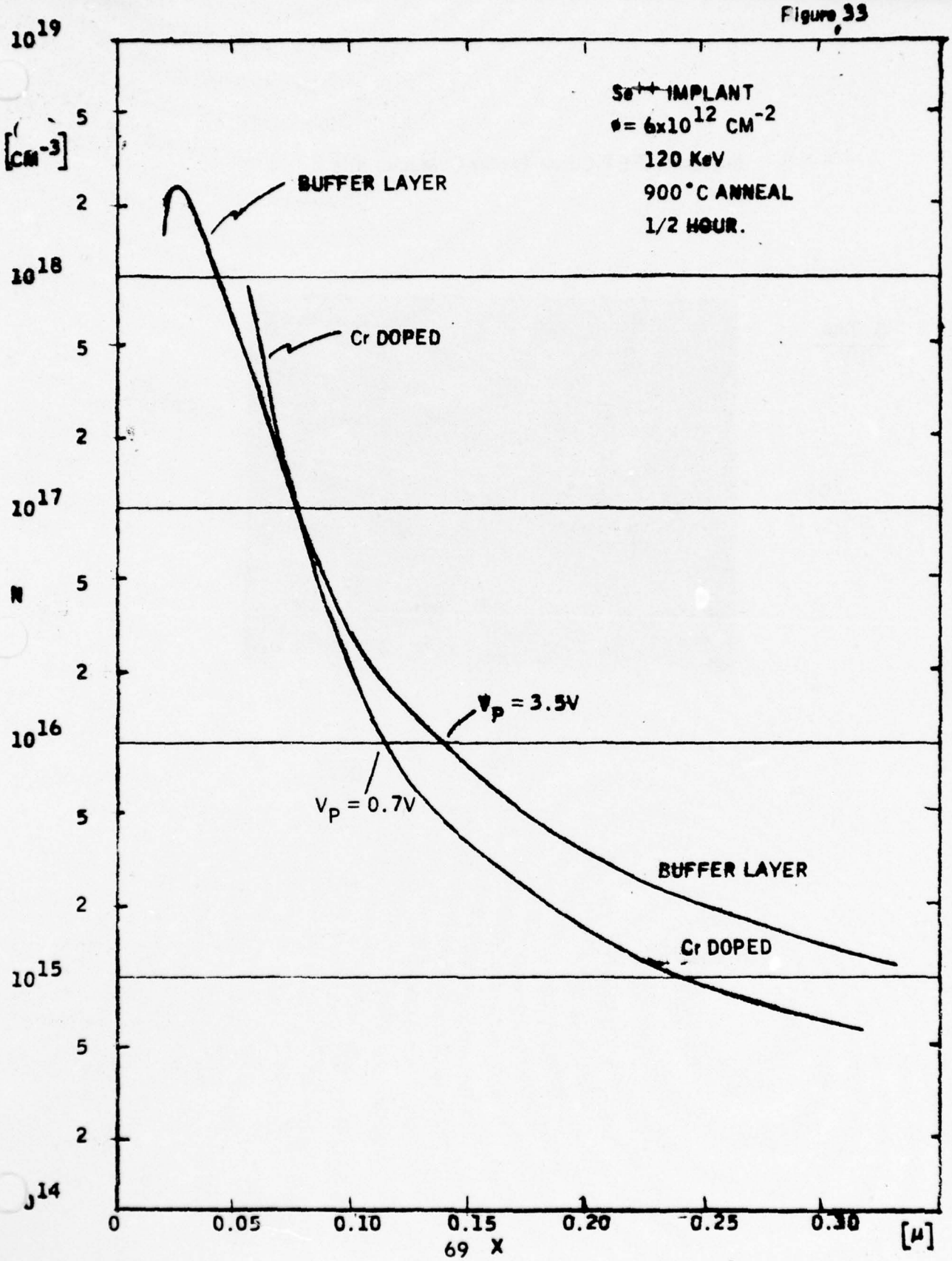
annealing temperature was increased, as evidenced by an increase in the zero-bias capacitance. The resulting profile after the 900°C anneal is shown in Figure 33. The Cr doped samples now show an implanted profile, but the pinch-off voltage is only 0.7V. This might have been predicted from Figure 31. Pinch-off voltage of the buffer layer sample has increased to 3.5V.

Table V presents a partial summary of characteristics of Se^{++} implants into Cr doped and buffer layer substrates. Characteristics were determined by Schottky barrier capacitance measurements.

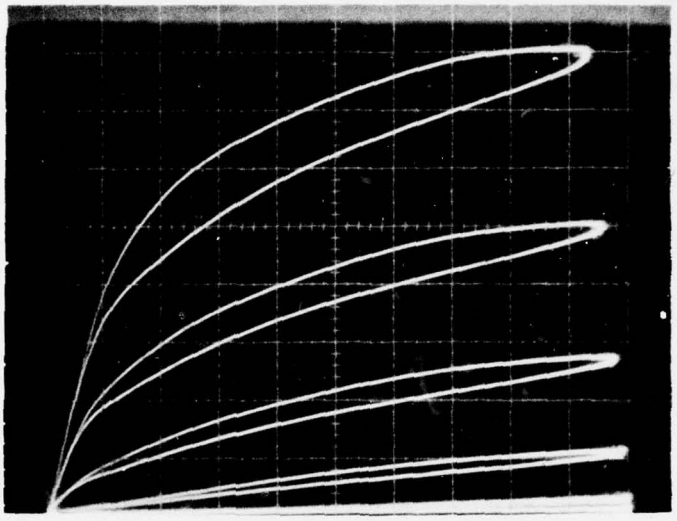
FETs were fabricated using buffer layer samples similar to that shown in Figure 33 which had been annealed at 900°C. Contacts were found to be fair, but the pinch-off voltage was considerably lower than had been determined by C-V plotting. The poor contact quality could be attributed to surface damage and/or surface doping. Reduction in the pinch-off voltage is not well understood, but etching does take place during the FET processing steps. This etching which is normally very slight may have been enhanced by damage or strain at the surface which was not completely annealed out.

Figure 34 shows the drain characteristics of the FETs. Maximum drain current I_{dss} = 1.8 mA, Gm = 3 mV, and V_p = 0.8V. Several additional implants were carried out varying the dose from $7X10^{12}cm^{-2}$ to $1X10^{12}cm^{-2}$, using Se^{++} at 60 KV. Doses greater than $6X10^{12}cm^{-2}$ caused the C-V data to breakdown at low voltage; well below the expected

Figure 33


Se++ IMPLANT
φ= 6x10^12 CM^-2
120 KeV
900°C ANNEAL
1/2 HOUR.
BUFFER LAYER
Cr DOPED
V_P = 3.5V
V_P = 0.7V
BUFFER LAYER
Cr DOPED
N
[CM^-3]
10^19
5
2
10^18
5
2
10^17
5
2
10^16
5
2
10^15
5
2
10^14
0
0.05
0.10
0.15
0.20
0.25
0.30
[μ]
69 X

Implanted FET Curve Tracer Characteristic



Run	Substrates	Implanted Q, cm^{-2}	Si_3N_4 Anneal	N_D Max cm^{-3}	V_p (Volts)
H-125	Cr	$5X10^{12}$ cm^{-2} 120 KeV	900°C 15 Min	$2X10^{18}$	~4V
H-126A	Buffer $N_D=8X10^{13}$ cm^{-3}	"	"	$2.5X10^{18}$	3.5
H-126B	Cr	"	"	$9X10^{17}$	0.7V
H-127	"	"	"	$5X10^{17}$	0.9V
107	"	$6X10^{12}$ 120 KeV	"	$2.5X10^{18}$	30V
Y-1700B	Buffer $N_D=10^{14}$ cm^{-3}	$5X10^{12}$ 120 KeV	"	$1X10^{18}$	1.6V
86A	Cr	$5.5X10^{12}$ 120 KeV	"	$2.5X10^{18}$	Break-down (V_p >14
86B	"	$5.0X10^{12}$ 240 KeV (Stanford)	"	----	Pinched off @ 0V
94-1	"	$1X10^{12}$ 120 KeV	"	----	"
94-2	"	$2X10^{12}$ 120 KeV	"	----	"
94-3	"	$3X10^{12}$ 120 KeV	"	----	"
94-4	"	$4X10^{12}$ 120 KeV	"	~ 10^{17}	~ 1V
102-4	"	$4X10^{12}$ 110 KeV	"	$2X10^{17}$	1.8V
3K-200A	Buffer $N_A=1X10^{15}$ cm^{-3}	$5.5X10^{12}$ 120 KeV	"	$3X10^{18}$	Break-down (V_p >1
3K-200B	"	$5X10^{12}$ 240 KeV (Stanford)	"	$5X10^{17}$	Break-down (V_p>1

TABLE V
Partial Run Summary, Se^{++} Implants
For GaAs FET Channel

pinch-off. Doses of less than $5X10^{-12}cm^{-2}$ gave pinch-off voltages of 1-2V before processing, and devices which were pinched off after application of the gate metal. Very slight etching of the wafer surface most frequently caused wafers which showed avalanche breakdown initially to have V_p of ~1-2V. Several attempts to fabricate FETs using 60 KV Se^{++} implants into Cr doped and buffer layer substrates resulted in devices with poor contacts, low Idss and low V_p.

(ii) Mobility Measurements -- Active Layers. Hall measurements were made on Se^{++} implanted layers in which the dose was $6X10^{12}cm^{-2}$, implanted at 60 KV. Si_3N_4 deposition and annealing were done as described earlier. Measurements were made using the standard Van der Pauw cloverleaf geometry. Contacts were a Ge-Au alloy with the pattern defined by photo masking. The cloverleaf pattern was defined by photomasking and etching away the implanted layer.

Table VI shows room temperature and liquid nitrogen mobility and doping for a $6X10^{12}cm^{-2}$ implant into a buffer layer substrate. Doping calculated from the Hall measurement is based on the assumptions that the film thickness is approximately twice the standard deviation or (~500Å). The average mobility under these conditions for these samples is about $2900\ cm^2V^{-1}sec^{-1}$.

Implants were also done into Cr doped qualified substrates with a total dose of $1X10^{13}cm^{-2}$. Hall data is shown in Table VI. Notable is the poor mobility and the fact that it is lower at

Run	Implanted Q, cm^{-2} Se^{++}	M_H 26°C	M_H 77°C
91A-4-1	$7.5X10^{12}$	2815	2614
91A-4-2	"	2717	2473
91A-4-3	"	2465	1923
91A-2-1	"	2143	2652
91A-2-2	"	3242	3447
91A-2-3	"	3240	3845
91A-2-4	"	2964	2666
91A-3-1	$1X10^{13}$	1856	1682
91A-3-2	"	1650	1490
91A-3-3	"	1632	1562
91A-3-4	"	1652	1417

TABLE VI

Hall Mobility of Se^{++} Implanted GaAs Wafers.
Implantation Energy = 120 KeV Annealed 900°C 15 Min.

liquid nitrogen than at room temperature, and the apparent lower electrical activity than observed in the buffer layer sample. The poor mobility may be due to the higher dose and presence of traps resulting from implanting directly into the Cr substrate.

c. Conclusions:

(i) Contact Implants. Sulfur implants were unsuccessful because of the equipment's inability to distinguish sulfur from oxygen ions. Selenium contact implants were obtained; however, FETs fabricated with such implants showed inferior characteristics to those without implanted contacts.

(ii) Annealing Cap. Considerable effort spent on developing a reproducible Si_3N_4 capping process has resulted in Si_3N_4 films which withstand annealing temperatures to 900°C. The process which previously gave films of variable quality and a pitted GaAs surface after annealing at 750°C now shows high reliability with improved Si_3N_4.

(iii) Substrate Qualification. A process has been developed for evaluating Cr doped substrates for suitability for use in making ion implanted FETs. The technique involves the measurement of surface breakdown voltage before and after a 900°C 1/2 hour anneal using an improved Si_3N_4 layer as a cap.

(iv) Active Layer Implants. Active layer implants have been done

using buffer layer and Cr doped substrates, but results are obtained using buffer layers and a 900°C anneal. The relationship between breakdown voltage and pinch-off voltage for these very narrow films makes it very difficult to achieve useful active layers. In addition, the mobility of these shallow films is low. Although FETs have been fabricated, their drain current and pinch-off voltage are very low. Implantation should be done at considerably higher accelerating voltage to achieve results which are comparable to those readily attained using epitaxially grown films.

(v) Hall Mobility-Active Layers. Hall measurements of Se^{++} ions implanted at 60 KV into buffer layer substrates show room temperature mobility of $\sim 3000\ cm^2_V{}^{-1}sec^{-1}$. Results are less encouraging for implants into Cr doped substrates. The reason for this could be related to trapping as a result of the Cr.

C. Test Samples

1. Test Procedures

It was required under this contract that Avantek deliver 6 groups of FET samples to demonstrate progress in device development. The Navy's use of the samples would include both performance tests and reliability tests. Thus, the optimum chip mounting system depended on the particular tests to be performed.

Avantek, therefore, made FET deliveries in two physical formats:

- A hermetically sealed package of cofired alumina/brazed construction. Usable to 10 GHz.

- An open carrier with input and output transmission lines. Usable to frequencies >20 GHz.

Figures 35 and 36 show the two mounting systems.

The hermetically sealed package is easiest to handle for most types of tests, but has an internal resonance in the 10 GHz range, thus limiting its usefulness to frequencies below 10 GHz. An open carrier has excellent frequency characteristics but requires very special handling since the FET is exposed. While the Avantek FET surface is protected by polycrystalline GaAs, the bonding wires themselves are still exposed and very fragile. An interim carrier design was used on one of the early deliveries (not shown) but was abandoned for the present design which has superior electrical performance. Testing of the Fet's included the following tests:

- DC - Standard

  I_{dss} , r_{do}, g_m, V_p

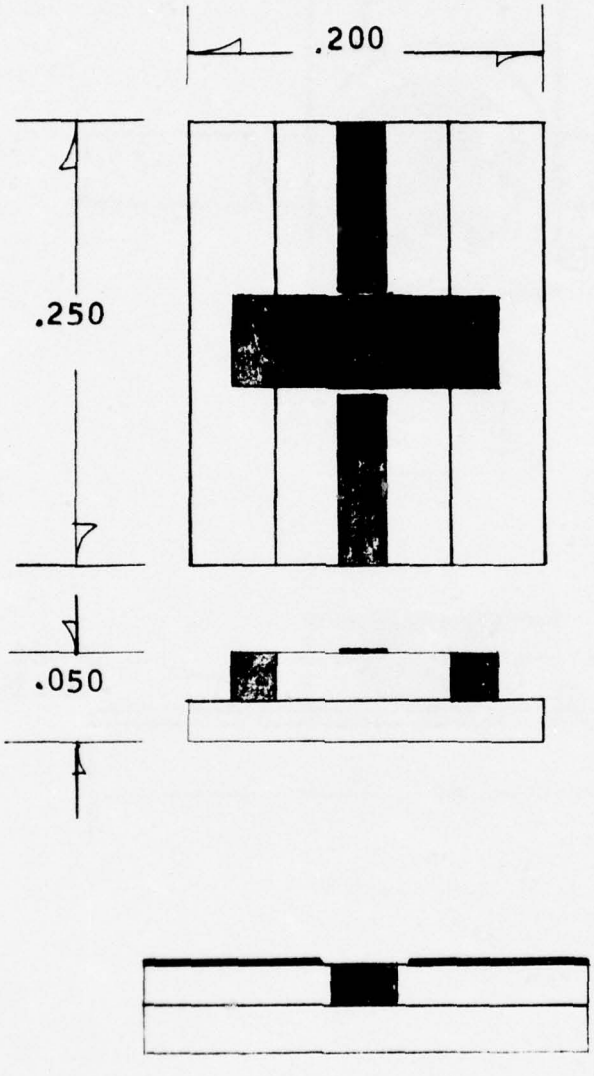
  DC - Special

  R_s, R_d, R_{gate}, C vs V, & Id, r_{dso}

- RF Tests

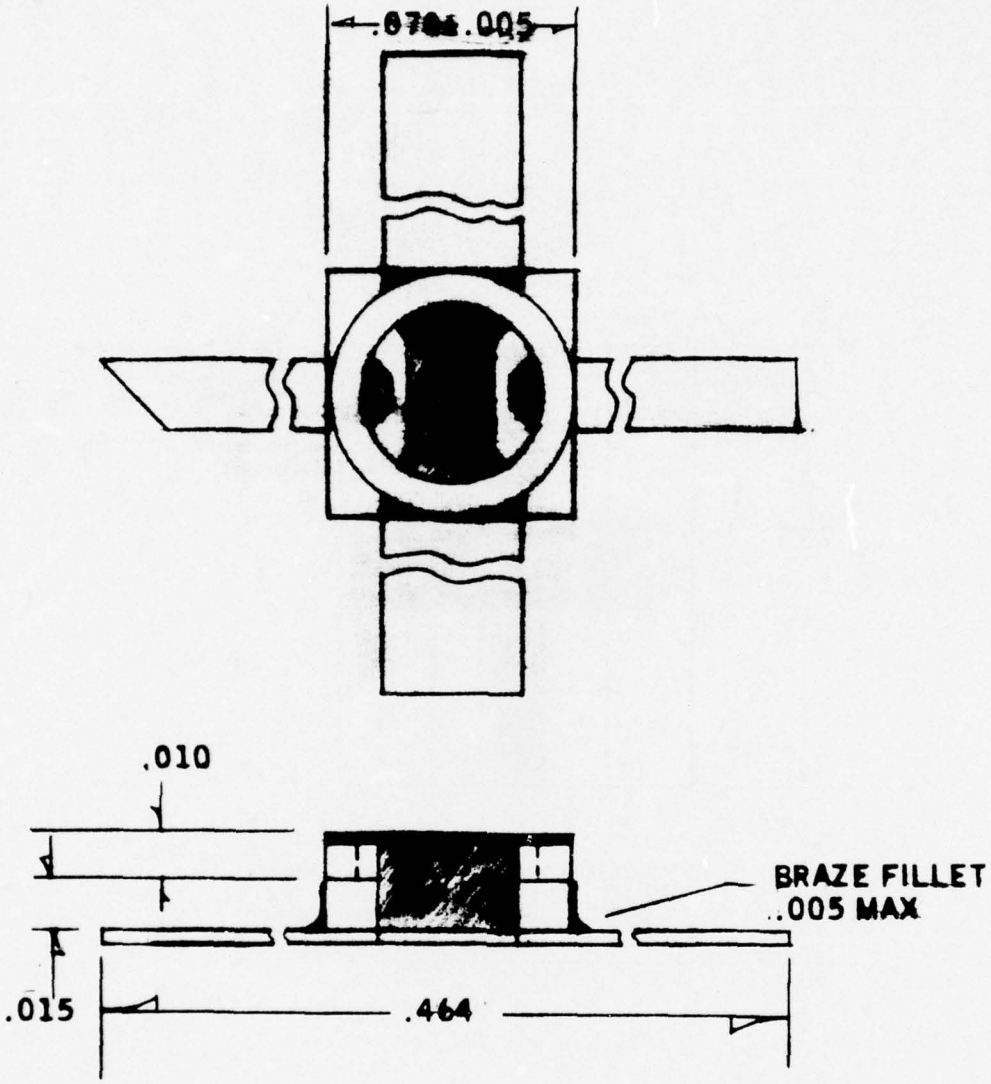
  Noise Figure & Gain at N.F. at 6, 10, and 18 GHz

  S-parameters 4-18 GHz at 10 ma, 20 ma



18 GHZ CARRIER
FIGURE 35

Figure 36



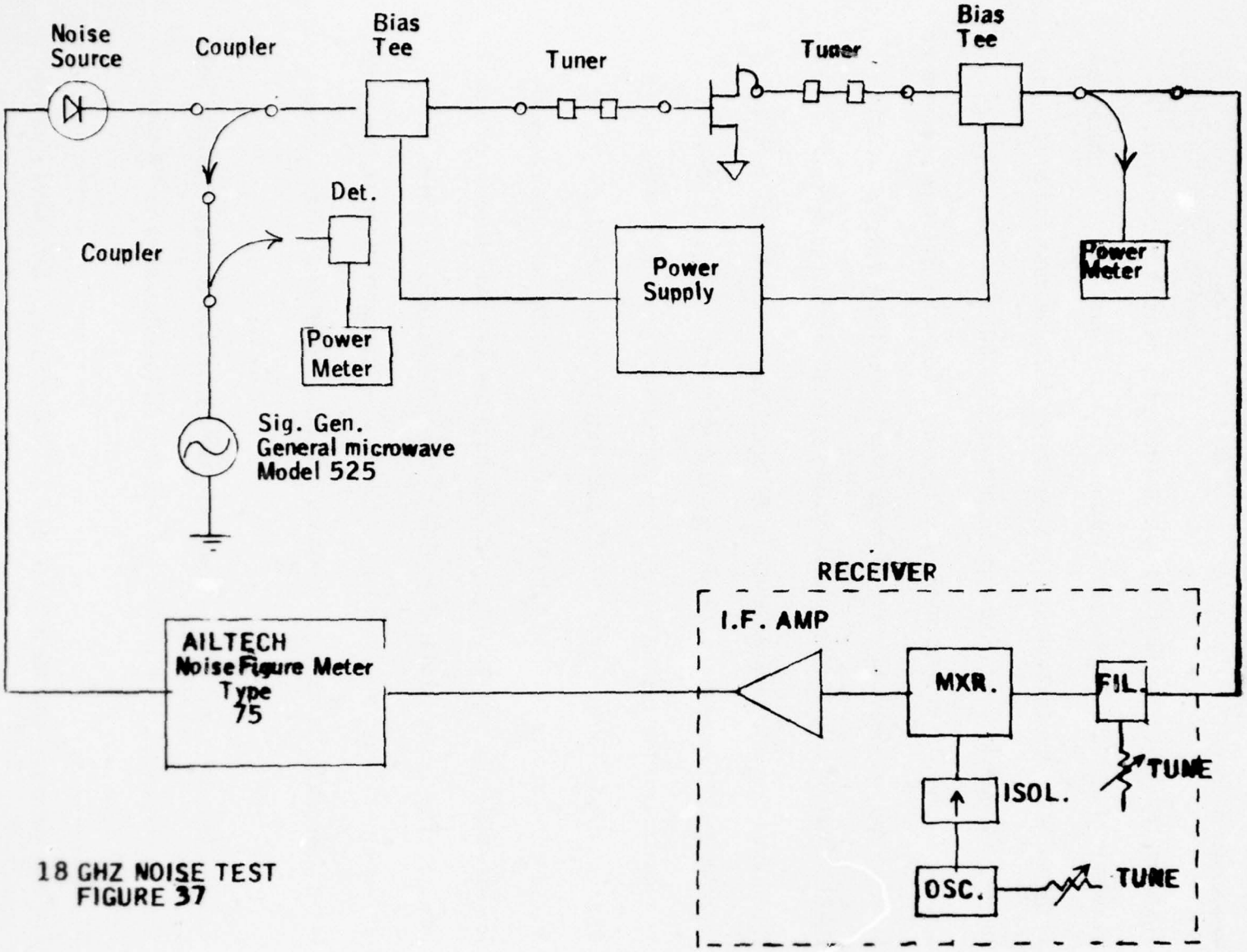
AVANTEK

STRIPLINE PACKAGE
70 MIL GaAs FET

A special test facility for Ku-Band was constructed to measure noise figure. A schematic of this layout is shown in Figure 37. Figure 38 is a photograph of the facility. In order to implement these tests, it was necessary to build special tuners. We were unable to find commercial tuners exhibiting low enough losses to be used for the type of measurements to be made. Coaxial slide-screw waveguide slide-screw, and sleeve tuners were investigated. The first two types are very complex mechanically and the second requires at least one waveguide/coax transition. Sleeve tuners turned out to be the easiest to construct and exhibited acceptably low losses at the VSWR's encountered in FET testing. Figure 39 is a photograph of one of the tuners. The internal slugs are made of brass with a silver plating (200 micro inches) and a gold flash to prevent tarnish. A teflon sleeve fits both over and inside the slug. In addition to providing the necessary low loss dielectric material, the teflon also functions as a low friction, low wear bearing. The transmission line itself is simply an Hewlett-Packard (HP), 10cm air line with a 3/32" slot milled in the side to allow movement of the sleeved slugs. In the photograph, the mechanical means for a vernier adjustment are also shown.

The bias tees are a specially selected pair manufactured by Hewlett Packard which show no resonances up to 18 GHz and only 0.2 dB loss (maximum) at 18 GHz.

The receiver block includes a Yig tuned 12-18 GHz filter, a Spacekom ultra low noise 12-18 GHz mixer, a Yig tuned Gunn oscillator tuning 12-18 GHz, isolators and an ultra low noise IF amplifier ($F \cong 1.3$ dB).



18 GHZ NOISE TEST
FIGURE 37

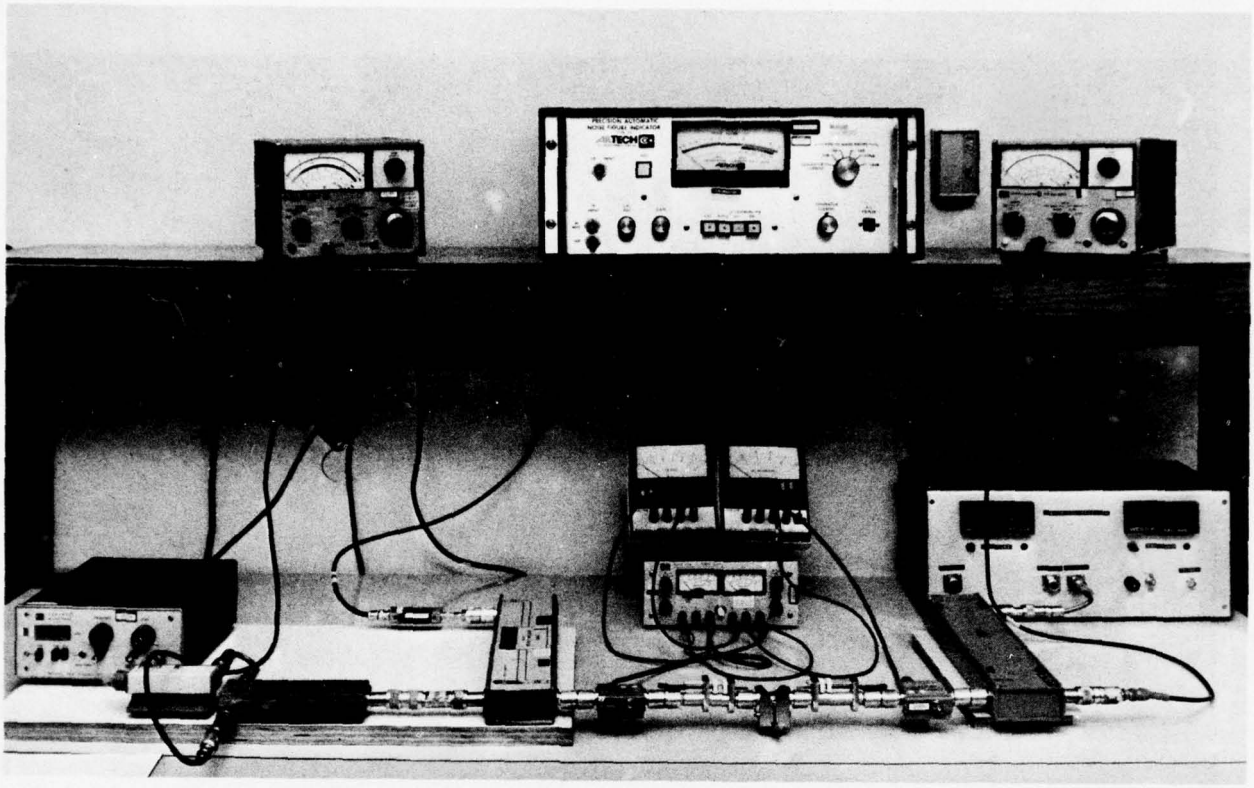


Figure 38. Photo of RF test facility for FET's.

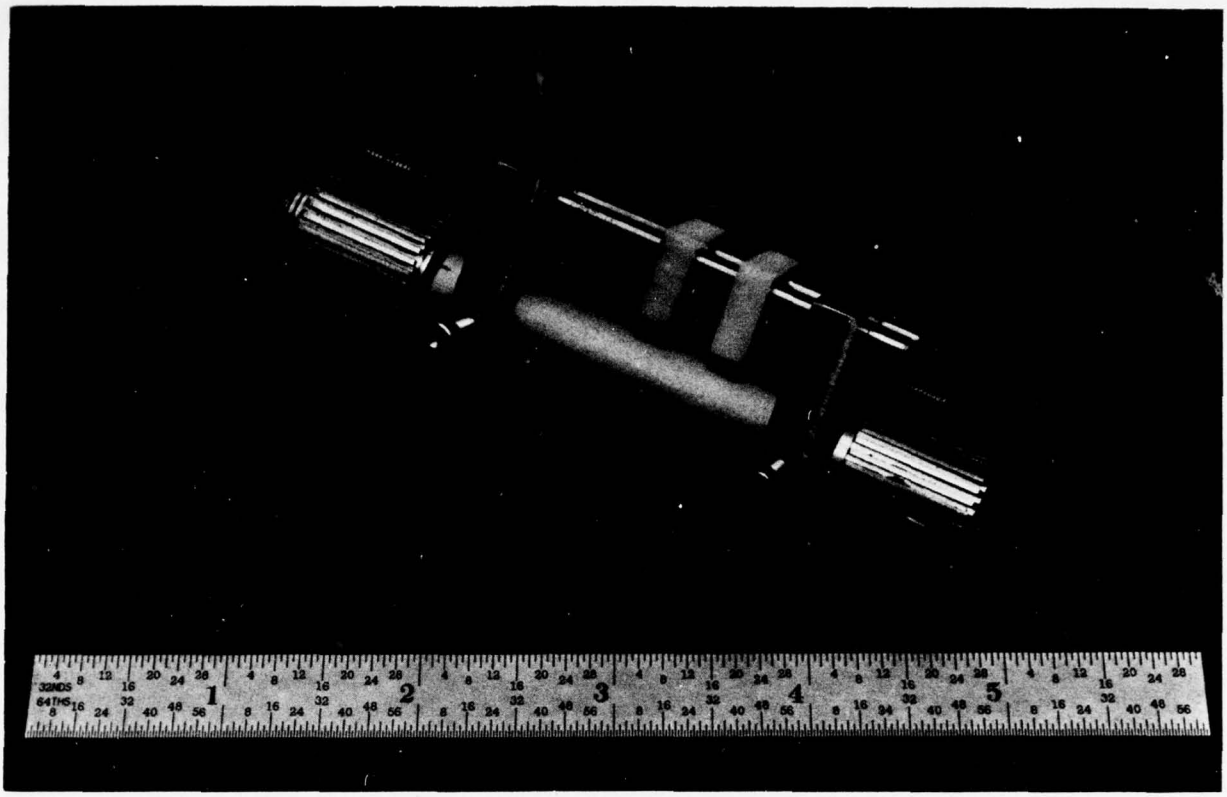


Figure 39. Sleeve/slug tuners for 1-18 GHz test.

In the external circuit, the couplers are HP 2-18 GHz low loss types. Couplers are used to introduce the CW test signal and extract it for gain measurement. Gain and noise figure can both be measured in this scheme. However, the CW signal must be off while the noise figure test is being made.

Typical parameters for this system at 18 GHz are as follows:

- Excess noise ratio of diode – 14.9 dB
- Input loss, diode to test fixture - 1.55 dB
- F_2 w/o fixture - 5.7 dB
- Test fixture loss - input, 0.2 dB
  output, 0.2 dB
- Corrected input loss - 1.75 dB
- Corrected F_2 - 5.9 dB

The test fixture itself is shown in Figure 40a. It has a fast load feature, but is otherwise similar to the one described in the circuit section.

2. Sample Data

Table VII summarizes the performance of the various samples. Note that the first three groups utilize the 1 micron geometry, and were delivered during the interval while Avantek was waiting for the first 1/2 micron mask. Exp 130B is the first sample using the 1/2 micron mask. The last sample, #6, uses the final 1/2 micron mask.

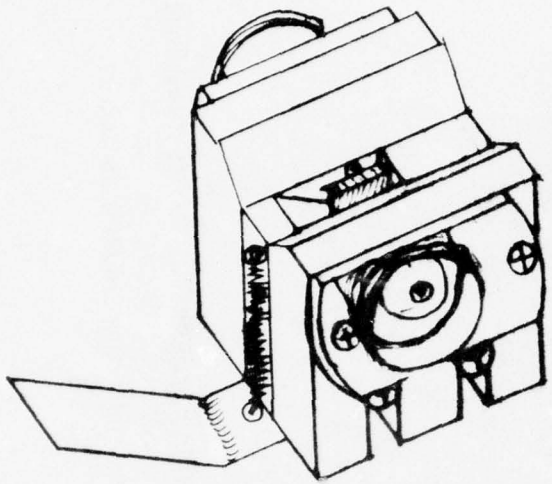


FIGURE 40a

TEST FIXTURE FOR 18 GHZ CARRIER

AD-A034 682 AVANTEK INC SANTA CLARA CALIF F/G 9/1
ANNUAL REPORT.(U)
NOV 76 N00014-75-C-1163
UNCLASSIFIED NL

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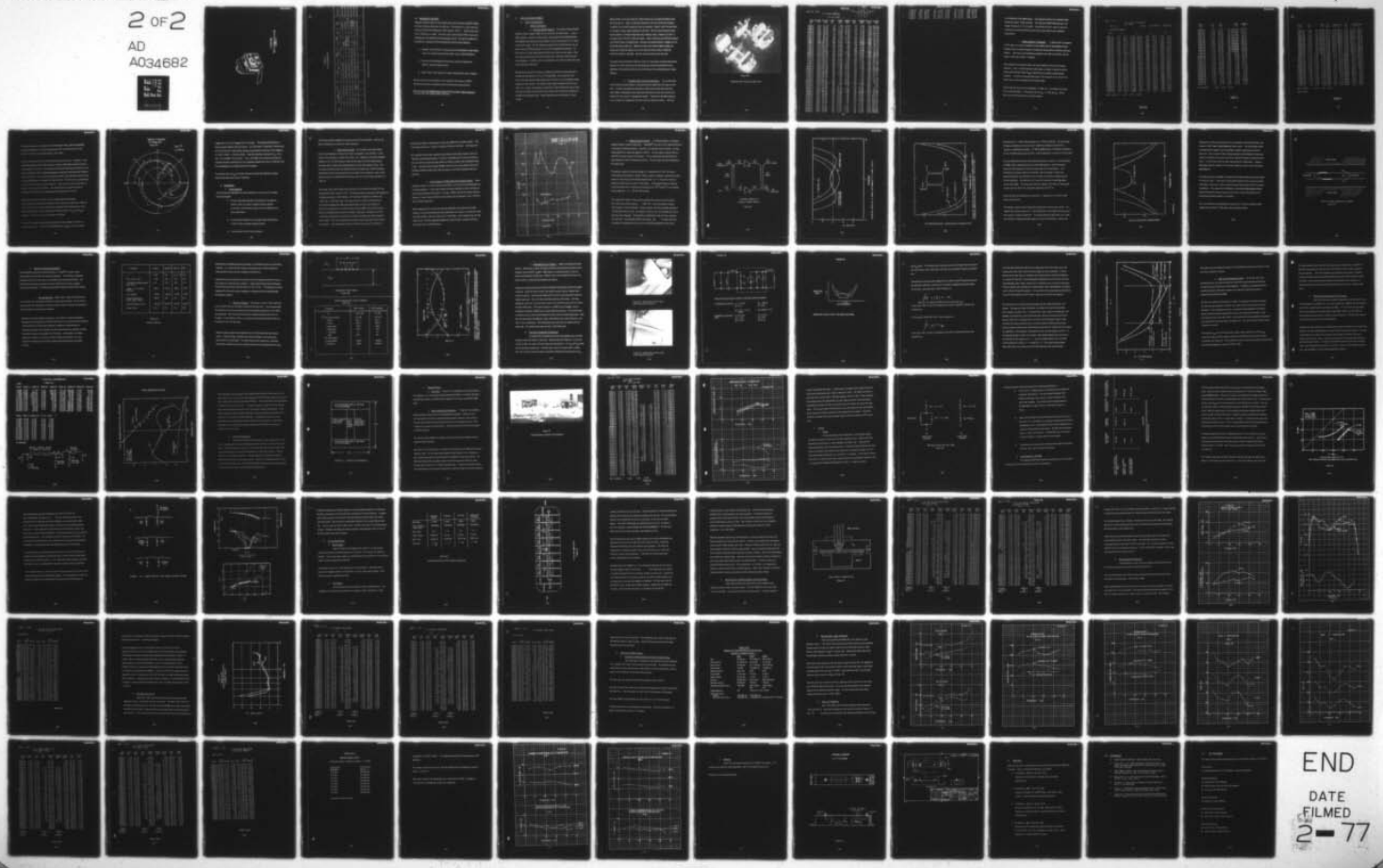

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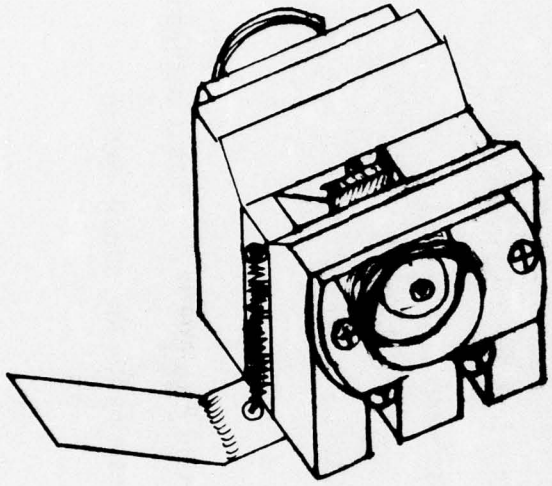


FIGURE 38a

TEST FIXTURE FOR 18 GHZ CARRIER

TABLE VII

FET TEST SAMPLE DATA

LOT NO.	Format		Mask	6 GHz		18 GHz		MAG		Slice Ident	Shipping Date
	Carrier	Pkg.		F	Gain	F	Gain	12	18		
1	--	10	1 μm	2.7-3.6	8.7-10.2					Exp 74c[1]	Sept. 17, 1975
2	--	10	1 μm	2.55-2.78	9.0-10.8	---	---	10 GHz 8.9-10.9	---	Exp 91A	Oct. 14, 1975
3	5	5	1 μm	2.3-3.5	8.5-10.7	---	---	Pkg. 4.1-8.2 *Carr.* 7.4-13.2	---	FET 205 APN	Dec. 16, 1975
4	10	-	.5μm	1.95-2.35	8.1-10.0	4.2-4.8	4.0-7.5	7.3	5.3	Exp 130B	Feb. 10, 1976
5	10	-	.5 μm	2.0-2.4	8.6-9.8	3.9-5.0	2.4-5.1	6.9-10.5	*	Exp 150B-1 Exp 159B	April 20, 1976
6	10	-	new .5 μm	2.4-2.8	7.3-9.5	---	---	7.5-8.1	6.2-6.7	Exp 179A	June 27, 1976

*Conditionally Stable, No Data

IV. RELIABILITY OF FETS

Although reliability testing is not a specific task under the present contract*, Avantek has been conducting these tests for some time. The latest test is a step stress test starting at 125°C and progressing in 25°C steps to 275°C. Dwell time for each step is 168 hours or 1 week. Tests will not be carried beyond 275°C since at this temperature the die separates from the package or carrier. No specific numbers can be quoted yet, although the following qualitative data have been observed:

- Between 125 and 225°C, some devices show improvement in gate leakage current and contact resistance while others show a slight degradation.
- Devices with high leakage are more prone to failure at temperatures >250°C, than low leakage devices.
- Above 250°C, gate leakage and contact resistance both begin to degrade.

Present fixturing is being upgraded to allow operation under bias up to 400°C.

The above test results were obtained with no electrical bias during the test.

*This is a task under ECOM Contract DAA B07-76-C-1300. Data is presented by permission of the ECOM Contract Supervisor.

V. AMPLIFIER DEVELOPMENT

A. Device Characterization

1. Scattering Parameters

a. Automatic Network Analyzer: Our Hewlett-Packard 8542A automatic network analyzer (ANA) was one of the last 'A' models made. It has a 2100 computer, cassettes, thermal printer, and keyboard like the 8542B models. The hardware and software have been updated so that in most respects our 'A' model is like the 'B' model. The 'B' models are supplied with an 8743 two-port test set while we have an 8746B four-port test set with a programmable attenuator. The 8743 test set is much simpler than the 8746 since it has only one coupler. However, during measurement, the input and output ports of the device under test must be interchanged. In addition, there is no attenuator in the 8743 to control the signal level to the device under test.

During the first year of this contract, our ANA was modified to extend operation to 18 GHz with the addition of a 12.4 to 18 GHz BWO. It was found that, for a 12.4 to 18 GHz manually swept signal input to the test set, the S-parameter output signals were not constant. The response of the coupler connected to Port 2 had a "hole" in it, in that the response was down about 7 dB for frequencies near 16 GHz. This hole at 16 GHz or other smaller holes did not seem to effect the calibration of the ANA in the automatic mode. Good calibrations now can be obtained through 18 GHz.

Below 15 GHz we use two of the HP 11605 flexible arms to connect the device under test to the test set. Above 15 GHz the attenuation of the HP 11605 arms increases, in general, but at certain frequencies there are attenuation "peaks" where the attenuation is too large to obtain a good calibration on the ANA. We have some data which shows that the phase of a "through" measurement may change by about 1 degree at 12 GHz if the rotary joints of the HP 11605 are rotated. Above 15 GHz we use 3/8 inch diameter semi-flexible cables (corrugated outer conductor and splined dielectric) between the test set and the device under test. When one of these semi-flexible cables is bent, the largest error introduced appears to be in the measured absolute angle of either the reflection coefficient or 'through'. We have some data which shows this error.

This phase error would directly effect the values of a linear phase deviation measurement. However, since the cables are not moved appreciably between measurements on two amplifiers, there should be little error in the difference of two measurements as in phase matching.

b. Transitions from 7mm Coax to Microstrip: To get useful data on FET devices and gain modules, good transitions are needed from 7mm coax to microstrip. A double step design was made and a number of these transitions were built. Figure 40bis a photograph of these transitions and shows how they may be used to test both the FET chip itself or a complete gain module. Table VIII is the ANA listing for a pair of transitions separated by 1/4 inch of 50 ohm ceramic microstrip. This data

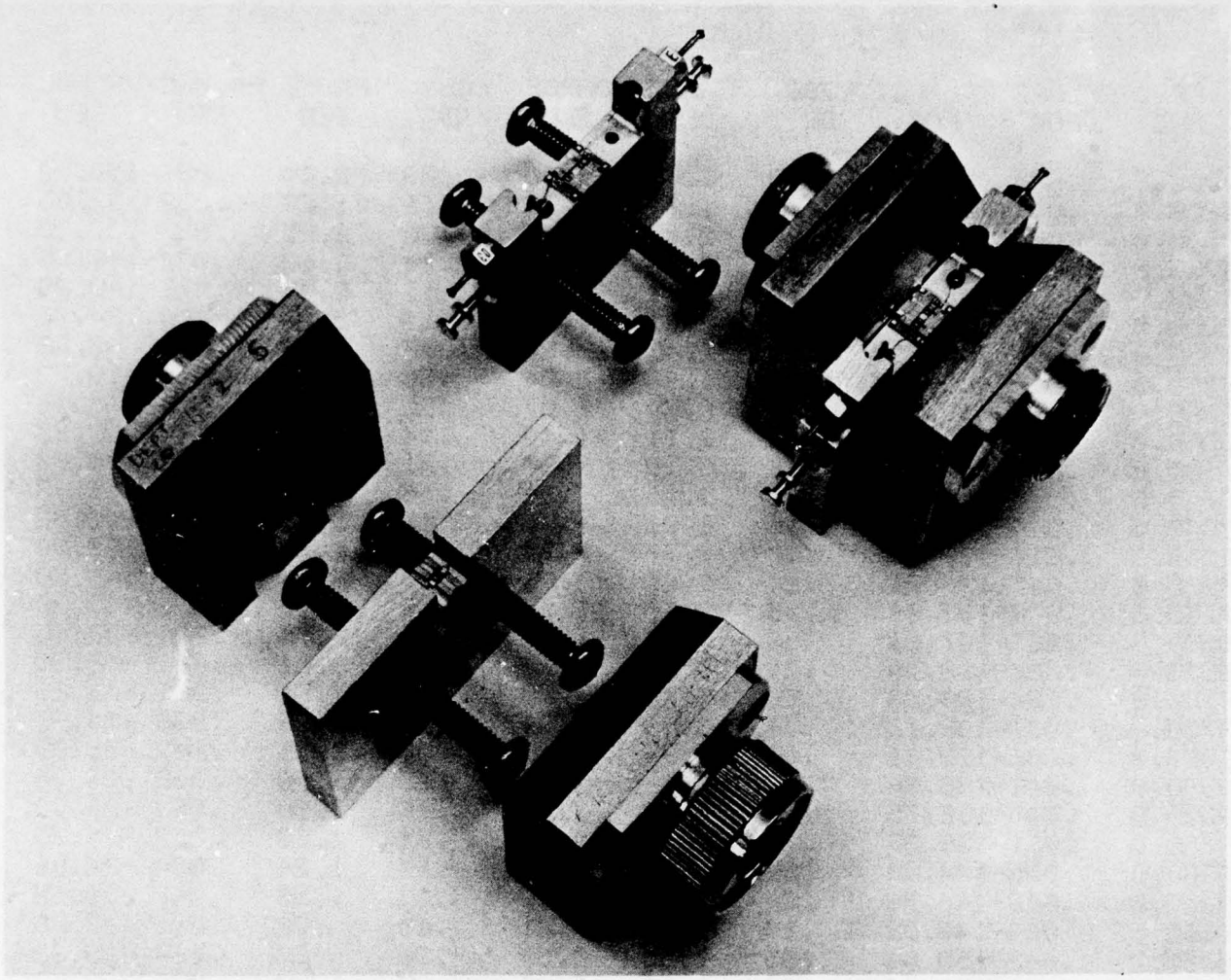
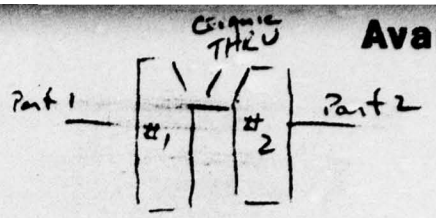


Figure 40b

Transitions from 7mm Coax to Microstrip

TABLE VIII



MAY 19, 1976

7-15 GAIN MODULES

S/N FIX THRU

FREQ MHZ	RFLMAG FOR	RFLANG FOR	LOSS DB	PHASE DEG	PHASE DEV	LOSS DB	PHASE DEG	RFLMAG REV	RFLANG REV
4000.0	.032	31.15	.10	2.08	-3.69	.09	2.04	.034	159.04
4250.0	.031	39.71	.12	1.79	-3.74	.11	1.77	.030	152.85
4500.0	.034	38.82	.20	2.49	-2.78	.20	2.25	.027	137.93
4750.0	.028	38.27	.14	2.63	-2.38	.14	2.63	.024	141.65
5000.0	.022	47.86	.14	2.52	-2.26	.11	2.45	.022	140.29
5250.0	.020	55.87	.16	2.91	-1.61	.15	2.66	.020	124.70
5500.0	.020	56.78	.16	3.45	-.80	.17	3.33	.013	97.82
5750.0	.014	68.71	.07	1.98	-2.04	.06	2.01	.010	119.73
6000.0	.006	82.88	.20	2.69	-1.07	.20	2.72	.006	116.10
6250.0	.003	137.51	.17	2.11	-1.40	.14	2.05	.004	57.23
6500.0	.006	-157.47	.22	3.19	-.07	.21	3.01	.003	23.13
6750.0	.010	-151.28	.11	3.13	.12	.10	3.38	.006	-52.38
7000.0	.014	-144.49	.16	2.69	-.06	.17	2.61	.009	-42.82
7250.0	.016	-136.41	.17	1.77	-.74	.20	1.72	.012	-39.34
7500.0	.017	-136.01	.24	2.65	.38	.24	2.68	.017	-41.09
7750.0	.018	-133.84	.19	3.17	1.17	.20	3.17	.020	-33.88
8000.0	.023	-127.26	.23	2.77	1.02	.19	2.76	.025	-32.46
8250.0	.026	-128.19	.21	2.28	.78	.21	2.51	.031	-32.39
8500.0	.026	-129.28	.20	1.47	.23	.18	1.64	.035	-29.23
8750.0	.031	-132.12	.36	2.83	1.84	.34	2.29	.039	-24.91
9000.0	.036	-132.61	.23	2.24	1.49	.20	2.11	.047	-25.98
9250.0	.041	-138.36	.28	2.38	1.89	.23	1.98	.052	-27.00
9500.0	.045	-138.75	.28	2.18	1.94	.26	1.60	.055	-27.36
9750.0	.051	-139.37	.30	2.32	2.34	.31	1.80	.059	-24.79
10000.0	.056	-144.00	.21	.82	1.08	.18	1.26	.064	-26.86
10250.0	.063	-146.70	.34	1.76	2.27	.33	1.53	.067	-30.55
10500.0	.064	-149.02	.29	.85	1.61	.25	.72	.065	-27.85
10750.0	.062	-150.00	.35	1.56	2.58	.30	.83	.064	-25.32
11000.0	.060	-150.50	.28	2.07	3.33	.29	1.79	.062	-23.67
11250.0	.060	-153.06	.25	.55	2.06	.25	.23	.057	-21.77
11500.0	.052	-156.44	.37	-.47	1.30	.28	-.59	.055	-19.68
11750.0	.050	-161.11	.32	.00	2.03	.33	-.44	.047	-16.33
12000.0	.046	-162.58	.38	.61	2.91	.38	.29	.039	-10.28
12250.0	.036	-176.40	.15	-.14	2.40	.13	-.27	.037	-5.95
12500.0	.029	177.60	.30	-.81	1.99	.27	-.49	.033	1.93
12750.0	.019	159.65	.28	-2.31	.74	.26	-2.18	.024	4.28
13000.0	.019	148.00	.44	-2.12	1.19	.32	-2.58	.022	-6.44
13250.0	.016	117.76	.23	-1.75	1.80	.31	-1.25	.011	20.70
13500.0	.015	105.34	.29	-2.42	1.39	.31	-2.34	.012	74.40
13750.0	.016	70.90	.28	-3.08	.97	.29	-2.82	.014	95.85
14000.0	.017	60.03	.30	-3.37	.92	.29	-3.30	.016	108.90
14250.0	.018	50.62	.26	-4.09	.46	.25	-3.79	.021	142.99
14500.0	.019	39.12	.33	-4.23	.58	.36	-4.30	.027	150.35
14750.0	.020	32.23	.32	-5.26	-.19	.29	-5.05	.032	152.22
15000.0	.020	34.67	.35	-5.06	.26	.36	-4.92	.031	156.09
15250.0	.019	33.70	.38	-4.58	.99	.39	-4.33	.027	156.17
15500.0	.027	14.17	.30	-6.53	-.71	.25	-5.89	.031	160.66
15750.0	.027	16.51	.39	-7.38	-1.31	.27	-7.43	.037	160.22
16000.0	.029	17.86	.36	-7.94	-1.64	.31	-7.66	.039	155.22
16250.0	.041	13.02	.39	-7.07	-.49	.38	-7.90	.040	148.38
16500.0	.039	29.63	.30	-8.11	-1.29	.32	-7.51	.042	153.00

16750.0	.051	33.54	.36	-9.41	-2.34	.34	-8.22	.048	132.29
17000.0	.067	32.40	.42	-10.91	-3.57	.32	-10.26	.055	122.09
17250.0	.072	35.09	.52	-9.94	-2.35	.44	-11.23	.066	124.91
17500.0	.085	39.61	.36	-10.72	-2.89	.52	-10.22	.064	95.72
17750.0	.099	45.90	.47	-10.84	-2.76	.42	-11.78	.080	92.11
18000.0	.119	52.42	.53	-12.24	-3.91	.42	-12.23	.089	68.88

is for transitions of the latest design. The measured insertion loss increased almost linearly up to about .5 dB at 18 GHz. The measured VSWR for the pair was 1.14 through 15 GHz and 1.27 to 18 GHz. Gold plated drill rod is used to contact the microstrip so that the transitions are physically strong enough to give repeatable measurements.

c. Measured Device S-Parameters: To obtain useful S-parameters on FET chips, the chips are mounted on metal carriers with the chip between 50 ohm microstrip lines on ceramic or quartz to simulate the actual physical mounting on the gain modules. Since there are no calibration standards for the ANA in microstrip, the calibration is done with the APC-7 standards.

After calibration, the reference planes are moved towards the chip by the following procedure. First, a 50 ohm section on either quartz or ceramic is placed in the test fixture and the through length of S_{21} is adjusted to give minimum variation around 0 degrees. A section of electrical length equal to the separation of the 50 ohm lines on the carrier is then subtracted from the through length.

Table IX thru XI show a set of S-parameters, K, MAG, etc., on a typical 1/2 micron device with joined gates. The bias was set at 3 V_{ds} = 3 volts and I_{ds} = 20 ma which was the typical bias used on the gain modules.

FEB 5, 1976

FET TEST .5 MICRON C1
EXP 1308

SER NO. 8 BIAS= 3.00 VOLTS, 20.00 MA

S -- MAGN AND ANGLES:

FREQ	11		21		12		22	
2000.00	.995	-18.5	1.552	162.6	.028	80.8	.740	-8.0
2500.00	.977	-22.4	1.548	158.3	.034	79.1	.743	-8.6
3000.00	.965	-26.2	1.540	153.7	.040	78.1	.735	-8.3
3500.00	.962	-29.6	1.570	149.0	.047	77.5	.726	-9.3
4000.00	.945	-34.2	1.540	146.5	.052	77.5	.723	-10.0
4500.00	.927	-38.9	1.555	141.2	.058	74.8	.722	-9.3
5000.00	.903	-44.5	1.561	135.6	.065	74.1	.708	-9.6
5500.00	.892	-49.4	1.569	132.4	.070	72.3	.695	-10.8
6000.00	.866	-56.7	1.565	127.6	.076	71.0	.694	-11.6
6500.00	.845	-62.2	1.565	121.9	.081	69.1	.679	-13.2
7000.00	.818	-68.0	1.543	116.9	.086	66.9	.663	-15.4
7500.00	.796	-72.9	1.516	113.3	.087	65.1	.653	-17.1
8000.00	.771	-79.9	1.531	108.4	.092	66.0	.643	-18.0
8500.00	.752	-85.1	1.488	104.3	.094	64.1	.636	-20.4
9000.00	.728	-91.1	1.465	98.7	.095	62.4	.626	-21.9
9500.00	.709	-96.6	1.459	95.3	.098	63.1	.618	-23.0
10000.00	.680	-104.1	1.433	90.8	.102	62.8	.607	-23.5
10500.00	.671	-109.8	1.380	87.5	.101	62.2	.598	-24.4
11000.00	.663	-115.3	1.377	82.5	.104	62.0	.585	-25.8
11500.00	.651	-121.4	1.352	79.0	.107	62.0	.573	-26.2
12000.00	.634	-126.7	1.311	75.3	.109	61.5	.570	-29.6
12500.00	.637	-131.0	1.302	73.0	.112	62.9	.569	-30.6
13000.00	.639	-136.5	1.317	68.0	.112	61.8	.542	-31.1
13500.00	.619	-143.0	1.264	64.1	.113	61.6	.522	-34.0
14000.00	.597	-148.1	1.256	61.5	.118	64.1	.525	-36.2
14500.00	.594	-154.8	1.263	58.2	.123	65.5	.503	-37.5
15000.00	.596	-160.4	1.238	52.7	.128	64.8	.500	-41.9
15500.00	.597	-168.1	1.227	48.4	.136	63.6	.484	-48.4
16000.00	.599	-174.1	1.200	43.1	.144	62.0	.460	-54.8
16500.00	.622	-179.4	1.172	38.9	.144	61.2	.475	-64.1
17000.00	.619	174.4	1.136	36.1	.148	60.2	.487	-69.2
17500.00	.603	171.3	1.090	30.5	.147	59.3	.474	-74.4
17999.99	.607	164.1	1.005	27.7	.147	57.4	.542	-83.5

REF PLANES = 2.90 2.90 5.80

TABLE IX

FREQ MHZ	S21 DB	MSG DB	K	MAG DB	MASON U DB
2000.00	3.82	17.46	.07	$$$$$$$	$$$$$$
2500.00	3.80	16.56	.24	$$$$$$$	26.84
3000.00	3.75	15.83	.34	$$$$$$$	23.39
3500.00	3.92	15.24	.33	$$$$$$$	31.01
4000.00	3.75	14.69	.38	$$$$$$$	29.12
4500.00	3.84	14.25	.48	$$$$$$$	22.09
5000.00	3.87	13.79	.58	$$$$$$$	20.81
5500.00	3.91	13.50	.59	$$$$$$$	20.93
6000.00	3.89	13.16	.64	$$$$$$$	20.53
6500.00	3.89	12.89	.71	$$$$$$$	19.43
7000.00	3.77	12.56	.79	$$$$$$$	17.51
7500.00	3.61	12.40	.88	$$$$$$$	15.81
8000.00	3.70	12.21	.90	$$$$$$$	16.92
8500.00	3.45	11.98	.96	$$$$$$$	15.60
9000.00	3.32	11.87	1.06	10.36	14.34
9500.00	3.28	11.73	1.09	9.94	14.42
10000.00	3.13	11.49	1.16	9.08	13.54
10500.00	2.80	11.35	1.24	8.42	12.52
11000.00	2.78	11.20	1.25	8.20	12.61
11500.00	2.62	11.00	1.29	7.79	12.13
12000.00	2.35	10.80	1.34	7.30	11.37
12500.00	2.29	10.67	1.29	7.46	12.11
13000.00	2.39	10.69	1.32	7.28	11.76
13500.00	2.04	10.49	1.47	6.44	9.98
14000.00	1.98	10.26	1.44	6.31	9.93
14500.00	2.03	10.11	1.41	6.28	9.97
15000.00	1.85	9.86	1.38	6.20	9.91
15500.00	1.77	9.54	1.31	6.20	10.17
16000.00	1.59	9.21	1.30	5.93	9.69
16500.00	1.38	9.10	1.20	6.37	10.63
17000.00	1.11	8.85	1.19	6.24	10.40
17500.00	.75	8.70	1.34	5.24	7.99
17999.99	.04	8.34	1.25	5.32	8.34
REF PLANES =	2.90	2.90	5.80		

TABLE X

FREQ MHZ	S21 DB	K	MAG DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000.00	3.82	.07	$$$$$$	20.4	4.5	307.4	3.45	276.0	126.2
2500.00	3.80	.24	$$$$$$	13.4	15.2	251.2	3.48	270.0	134.0
3000.00	3.75	.34	$$$$$$	11.6	17.5	213.8	3.37	268.7	123.1
3500.00	3.92	.33	$$$$$$	11.3	14.8	188.3	3.26	251.1	125.1
4000.00	3.75	.38	$$$$$$	9.73	16.1	160.9	3.21	242.3	127.0
4500.00	3.84	.48	$$$$$$	8.54	16.8	140.0	3.20	248.9	120.8
5000.00	3.87	.58	$$$$$$	7.33	17.6	120.2	3.02	237.7	111.9
5500.00	3.91	.59	$$$$$$	6.91	16.1	106.8	2.87	219.4	111.2
6000.00	3.89	.64	$$$$$$	6.03	15.6	90.5	2.85	212.6	114.5
6500.00	3.89	.71	$$$$$$	5.43	15.5	80.7	2.69	194.0	111.7
7000.00	3.77	.79	$$$$$$	4.81	15.6	71.8	2.52	174.1	109.2
7500.00	3.61	.88	$$$$$$	4.36	15.7	65.3	2.41	161.0	107.5
8000.00	3.70	.90	$$$$$$	3.92	15.3	57.4	2.32	153.9	104.5
8500.00	3.45	.96	$$$$$$	3.62	15.1	52.1	2.25	140.4	104.6
9000.00	3.32	1.06	10.36	$$$$	4.5	40.2	$$$$$	31.4	129.2
9500.00	3.28	1.09	9.94	$$$$	5.2	36.3	$$$$$	35.7	127.6
10000.00	3.13	1.16	9.08	$$$$	6.5	31.4	$$$$$	47.0	124.9
10500.00	2.80	1.24	8.42	$$$$	7.3	28.4	$$$$$	53.8	120.4
11000.00	2.78	1.25	8.20	$$$$	7.2	25.5	$$$$$	52.6	115.2
11500.00	2.62	1.29	7.79	$$$$	7.4	22.3	$$$$$	55.7	113.3
12000.00	2.35	1.34	7.30	$$$$	7.8	19.8	$$$$$	53.3	107.5
12500.00	2.29	1.29	7.46	$$$$	6.9	17.9	$$$$$	48.6	109.4
13000.00	2.39	1.32	7.28	$$$$	7.0	15.6	$$$$$	50.7	102.6
13500.00	2.04	1.47	6.44	$$$$	8.1	12.9	$$$$$	53.9	94.4
14000.00	1.98	1.44	6.31	$$$$	8.1	10.7	$$$$$	51.3	95.3
14500.00	2.03	1.41	6.28	$$$$	7.7	8.2	$$$$$	50.2	93.7
15000.00	1.85	1.38	6.20	$$$$	7.3	5.9	$$$$$	43.3	89.0
15500.00	1.77	1.31	6.20	$$$$	6.6	3.1	$$$$$	35.4	82.8
16000.00	1.59	1.30	5.93	$$$$	6.4	1.0	$$$$$	31.2	74.8
16500.00	1.38	1.20	6.37	$$$$	5.0	-.7	$$$$$	21.4	69.1
17000.00	1.11	1.19	6.24	$$$$	4.8	-3.0	$$$$$	18.6	66.1
17500.00	.75	1.34	5.24	$$$$	6.4	-4.2	$$$$$	21.7	59.1
17999.99	.04	1.25	5.32	$$$$	5.5	-6.6	$$$$$	14.3	54.9

REF PLANES = 2.90 2.90 5.80

XTR2C-READY

TABLE XI

The reference planes are at the ends of the 50 ohm quartz lines, and the S-parameters include the inductances of the wires connecting the FET to the 50 ohm quartz lines. Figure 41 shows the S-parameters plotted in polar format.

The wires connecting the FET to the 50 ohm microstrip are 0.5 mil in diameter. A wire connecting the gate or drain to the microstrip is about 0.025 inches long and will have a self inductance of 0.55 nH. Two of the wires connect the joined gate to the 50 ohm microstrip, so that their combined inductance depends on their mutual inductance and is between 0.28 and 0.55 nH. Three such wires connect the drains to the 50 ohm microstrip so that the combined inductance is between 0.18 and 0.55 nH. The FET source is grounded with two 0.01 inch wires without mutual inductance. Each source wire has an inductance of about 0.16 nH or together 0.08 nH. The step that the die are mounted on has an inductance of 0.03 nH giving a total common lead inductance of 0.11 nH.

One of the uses of the parameters is in the computer aided design program used to simulate the actual circuit so that the circuit values can be optimized. When the circuit values from the computer program were compared to the actual optimized circuit, there were differences which indicated that the measured angles, of S_{11} and S_{22} in particular, could be wrong by about 10 degrees at 15 GHz.

The errors in the measured parameters are mostly due to the imperfect 7 millimeter to microstrip transitions. As seen in Table VIII, the angle of S_{21} for a 50 ohm through -

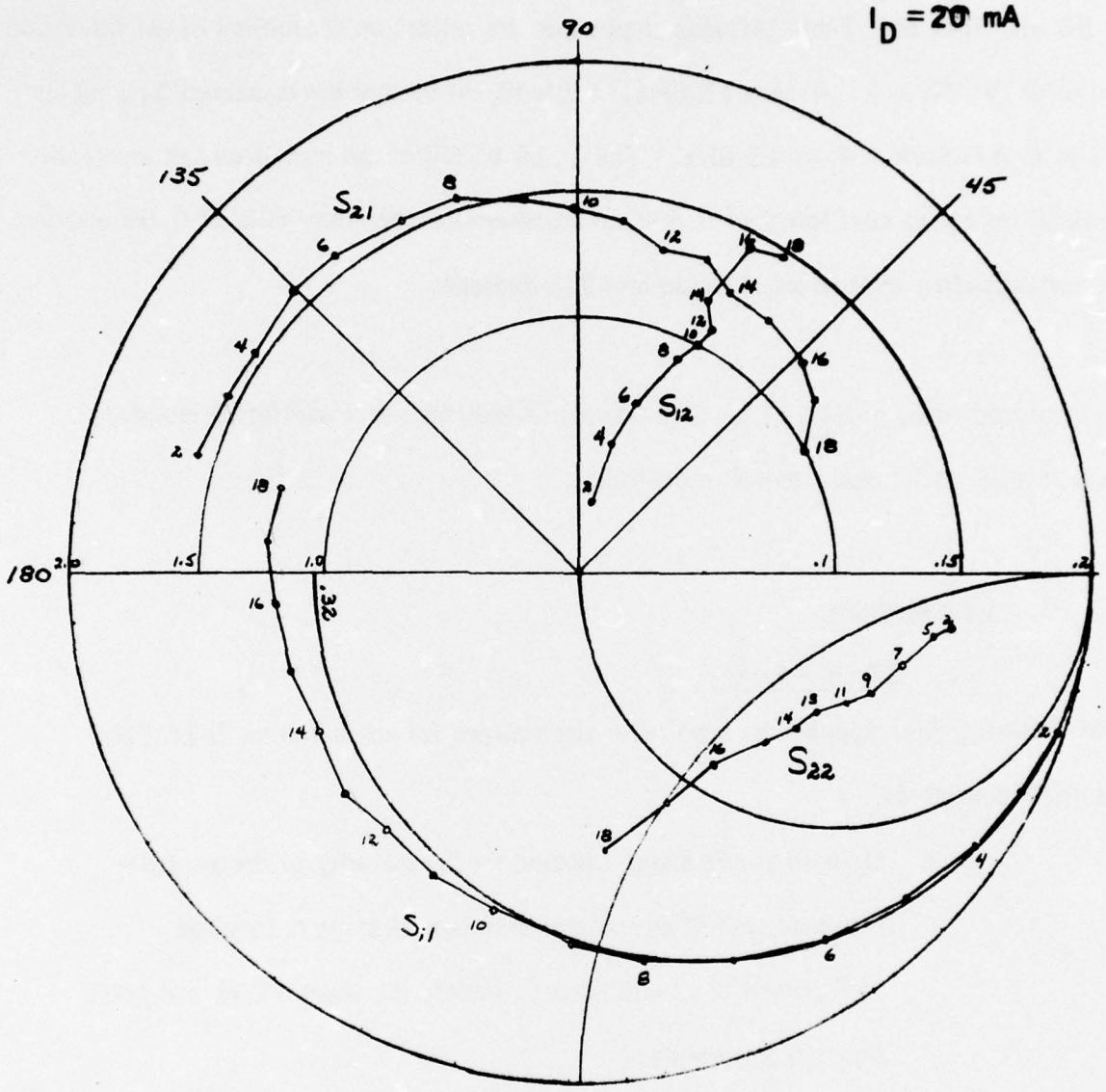
Measured S-Parameters

1/2 Micron FET

Figure 41

$V_{DS} = 3V$

$I_D = 20$ mA



changes from +2 to -2.5 degrees from 7 to 15 GHz. The angle of the reflection coefficient would change by twice this amount. This error makes it impossible to define where the 50 ohm lines end. Table VIII also shows that the reflection coefficient of the transition is 0.067 (VSWR = 1.14) thru 15 GHz. Table IX shows that the measured S_{11} on the FET is 0.6 (VSWR = 4) at 15 GHz. The 1.14 VSWR of the transition can cause the measured reflection coefficient of 0.6 to be anywhere between the limits of 0.55 and 0.64. The corresponding error in angle would be ±2.5 degrees.

The measured value of S_{12} at 14 GHz and above indicates that additional isolation between input and output circuits is desirable.

B. Gain Modules

1. Design Approach

The following three approaches are viable alternatives for achieving an 7-15 GHz amplifier bandwidth.

- Using a single ended cascade for the majority of the amplifier. However, either an isolator or balanced stage is required at the input to simultaneously satisfy the input VSWR and noise figure requirements.

- Using isolators between one or two stage single ended modules in order to buffer interstage matching problems.

- Using balanced amplifier design throughout.

The balanced amplifier approach was chosen as being the most practical. However, the other two approaches are worthy of a short discussion.

a. Single Ended Cascades: The cascading single ended stages has obvious advantages in reducing the number of components in the amplifier. It also results in less complexity, smaller size, weight, etc. Experience with octave bandwidth amplifiers in the 2-4 GHz frequency range has also proven that single ended designs have better phase linearity than balanced designs over the same frequency range. This is because the hybrids used in the balanced design or isolators have a definite bandpass characteristic and thus have phase pulling at the edges of their passband. Using a large number of either in an amplifier design obviously gives "N" times the phase deviation of a single one.

A two stage single-ended module using the present 1 micron production GaAs FET was fabricated and tested in August 1975. The matching elements consisted of both lumped and distributed elements on .025" alumina. The total area including bias networks was .330" long x .200 inches wide. By using a shunt R-L network to feed the drains, the interaction between the stages was dampened down so that a gain response of 8±1 dB was obtained from 7 to 15 GHz with an output VSWR of less than 2:1 when a choke was substituted for the shunt R-L networks. More gain (~12 dB@7 and 12.4) could easily be obtained but with a dip of 1-2 dB at 9-10 GHz and a large increase in output VSWR. Two of these modules were cascaded to give a post amp for noise figure measurements. The cascade had a minimum of 20 dB of gain from 7-12.4 GHz but

had excessive ripple (≈9 dB) because of ripple and VSWR of the individual stages. The noise figure varied from 7.0 dB at 7.0 GHz to 8.0 dB at 12.0 GHz. (See Figure 42)

We concluded from the above experiment that although single ended cascades could give impressive gain bandwidth numbers, it would be exceedingly hard to control gain flatness and, to be able to cascade any large number of modules to obtain octave bandwidths above 7 GHz. Also both input and output VSWR's would also have to be reduced by the use of isolators or balanced stages at the input and output if noise figure and power were to be preserved.

b. Using Isolators for VSWR and Buffering Between Stages: Single resonance isolators in X and Ku-Band are reasonable in size and have good performance up to octave bandwidths. These same isolators have been stretched to cover 8-18 GHz but with somewhat degraded performance (1.4:1 Max. VSWR's and 16 dB minimum isolation). However, it seems unlikely that these same isolators can be stretched to cover 7-18 GHz with acceptable performance.

Another approach which can give the necessary bandwidth is the edge guided isolator. However, it has the disadvantage of being complicated, much larger in size than the single resonance isolators, and has losses in the 1.5 dB range. Either approach does not seem viable for the 7-18 GHz bandwidth although the single resonance isolators could have been useful in the 7-15 GHz design.

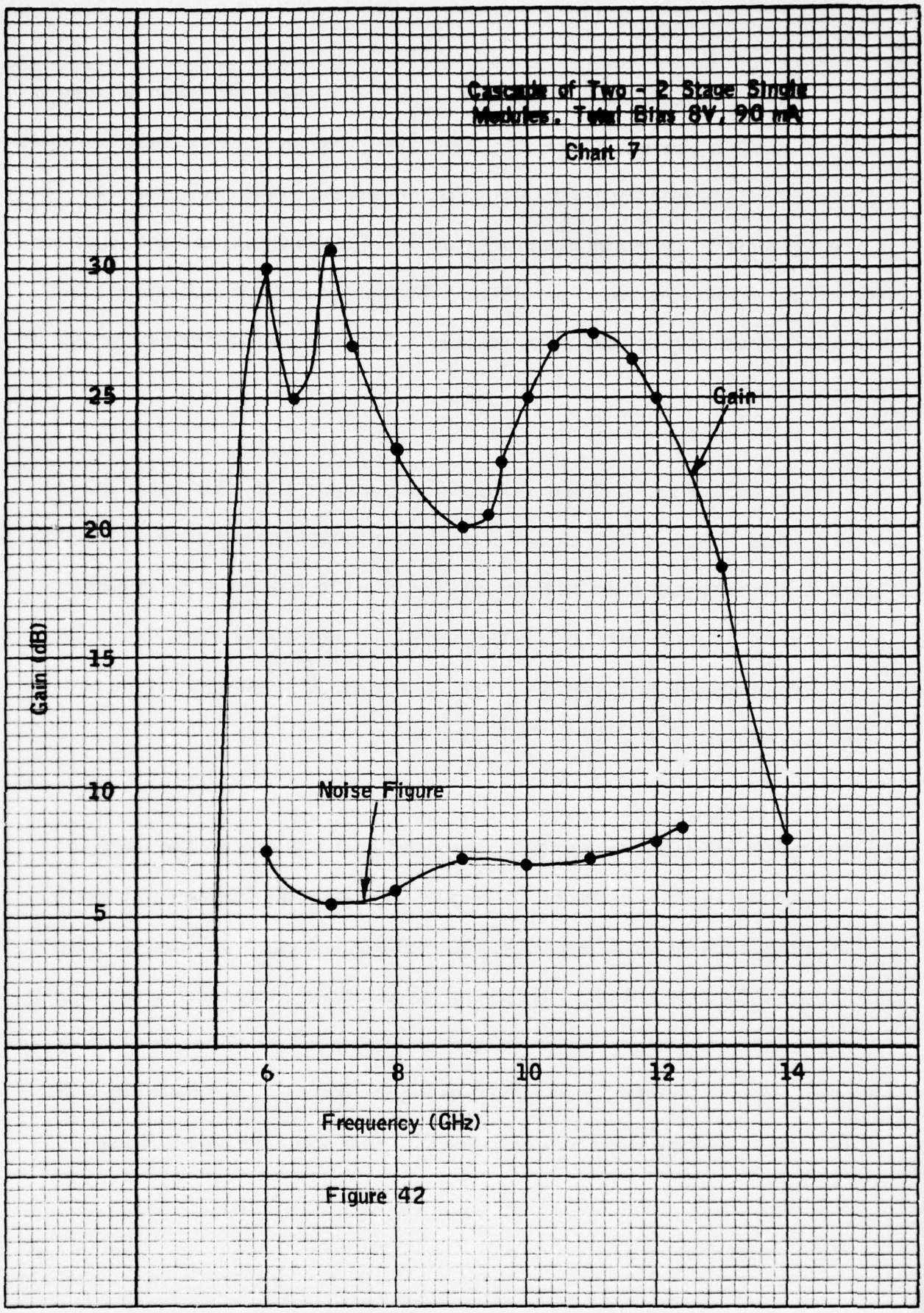
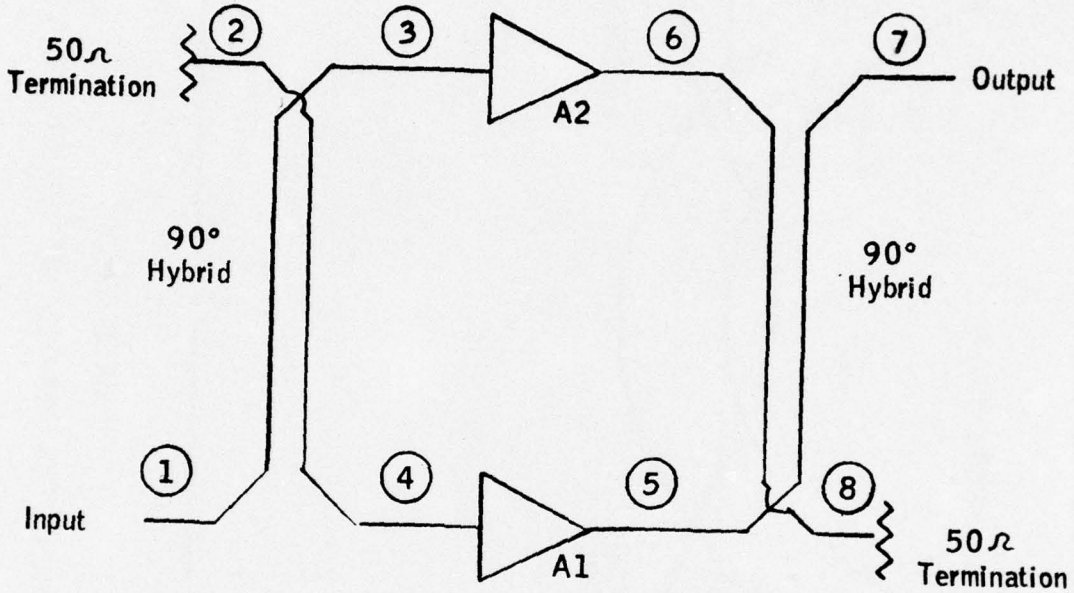

Cascade of Two - 2 Stage Single Modules. Total Bias 8V, 90 mA
Chart 7
30
25
20
15
10
5
Gain (dB)
Gain
Noise Figure
6
8
10
12
14
Frequency (GHz)

Figure 42

c. Balanced Amplifier Design: A schematic diagram of a balanced amplifier module is shown in Figure 43. Kurokawa[5] has given a very complete discussion of the theory of balanced amplifiers. Basically, the technique works as follows: An input signal applied at 1, splits and appears at 3 and 4. The two signals at those points are now 90° out of phase because of the hybrid. The two signals are then amplified by A1 and A2 which are made as identical as possible. The two signals are then recombined by the output hybrid.

The phasing is again such that they appear at 7 in phase and at 8 180° out of phase. If the coupling of the hybrids is exactly 3 dB at a particular frequency, then the two signals cancel at 8 and the gain of the balanced amplifier from 1 to 7 is that of the individual stages A1 and A2 minus any losses in the hybrids. At frequencies where the coupling is not 3 dB, there will be a reduction in gain equal to $2k\sqrt{1-k^2}$ where k^2 is the coupling of the coupled port ($k = .707$ for 3 dB coupling).

The simplest 90° hybrid is one section of coupled lines with an electrical length of 90° at the design center frequency. Figure 44 gives the frequency response of the coupled arm for two different 1 section couplers, one with a mid-band coupling of 3.0 dB and the other 2.4 dB. All couplers, of course, have zero coupling at dc and at twice the center frequency. The deviation of coupling from 3 dB will cause mismatch loss and ripple in the balanced amplifier (See Figure 45). A coupler with 3 dB of coupling at midband works very well over a 30-40% bandwidth but would cause



Schematic Diagram of a
Balanced Amplifier Module

Figure 43

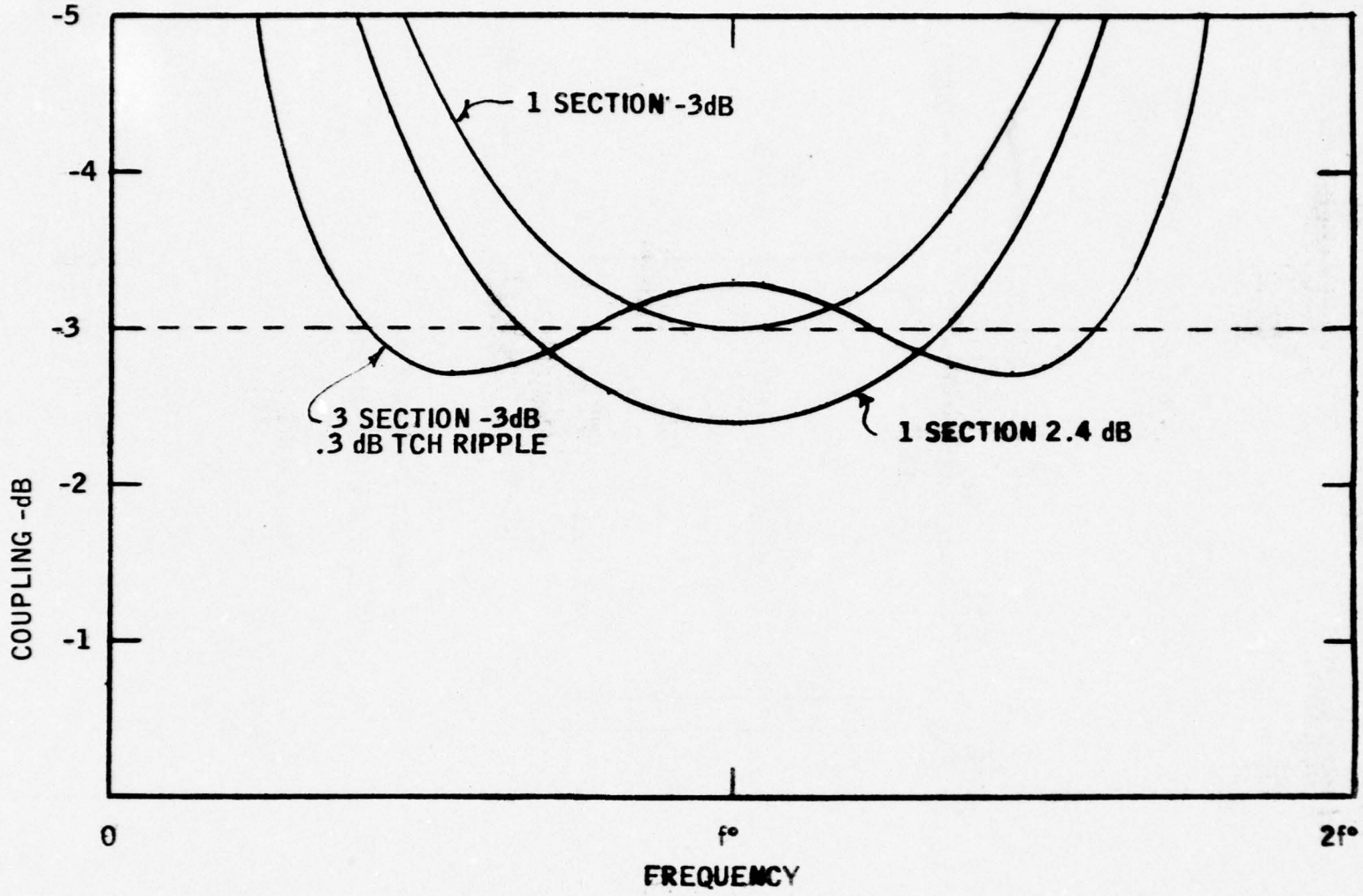


FIGURE 44 COUPLING vs FREQ. FOR VARIOUS 90° HYBRID DESIGNS

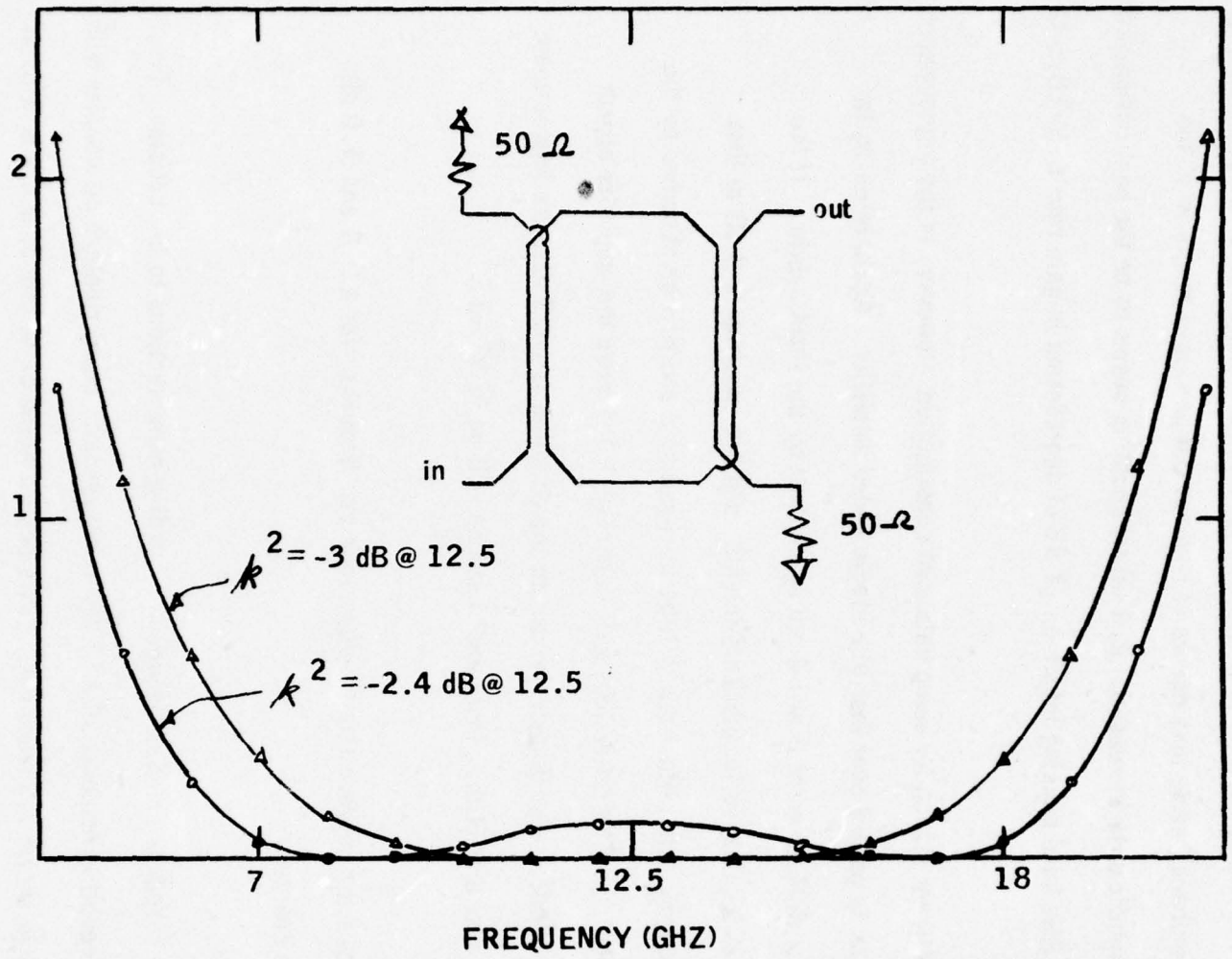


FIGURE 45 THROUGHT LOSS FOR 2-1 SECTION 90° HYBREDS CONNECTED IN BALANCED CONFIGURATION (ELECTRICAL LENGTH = 90° @ 12.5 GHZ)

significant loss (≈ .3 dB) at the band edges of a 7-18 GHz amplifier. By overcoupling the design at midband, some loss occurs at midband but bandpass response of the amplifier is significantly increased. 2.4 dB ou coupling seems to be the best compromise for the 7-18 GHz band causing less than .1 dB of degradation in gain from 6.5-18.5 GHz.

The most significant reason for using balanced construction, however, is the improvement in VSWR which is gained over that of a single ended amplifier. Again referring to Figure 43, any reflections at 3 and 4 are again split by the input hybrid. If the amplifiers have identical reflection coefficients, and the coupling is 3 dB at that particular frequency, the reflections will be in phase at 2 and will be absorbed by the 50 ohm termination. The reflections will cancel at 1 and make the amplifier appear to have unity VSWR. For frequencies where the coupling is not 3 dB, the improvement in return loss over that of the single ended stages will be $(2k^2 - 1)$.

Figure 46 shows the improvement in return loss vs frequency for a 2.4 and 3.0 dB single section coupler.

The frequency response could be improved by adding more sections to the coupler. For example, the coupling response of a .3 dB Tchebyscheff, equal ripple,3 dB coupler with three sections is shown in Figure 44. This design would be usable over a 4 to 1 band and would give an appreciable safety margin over a one section design. However, the

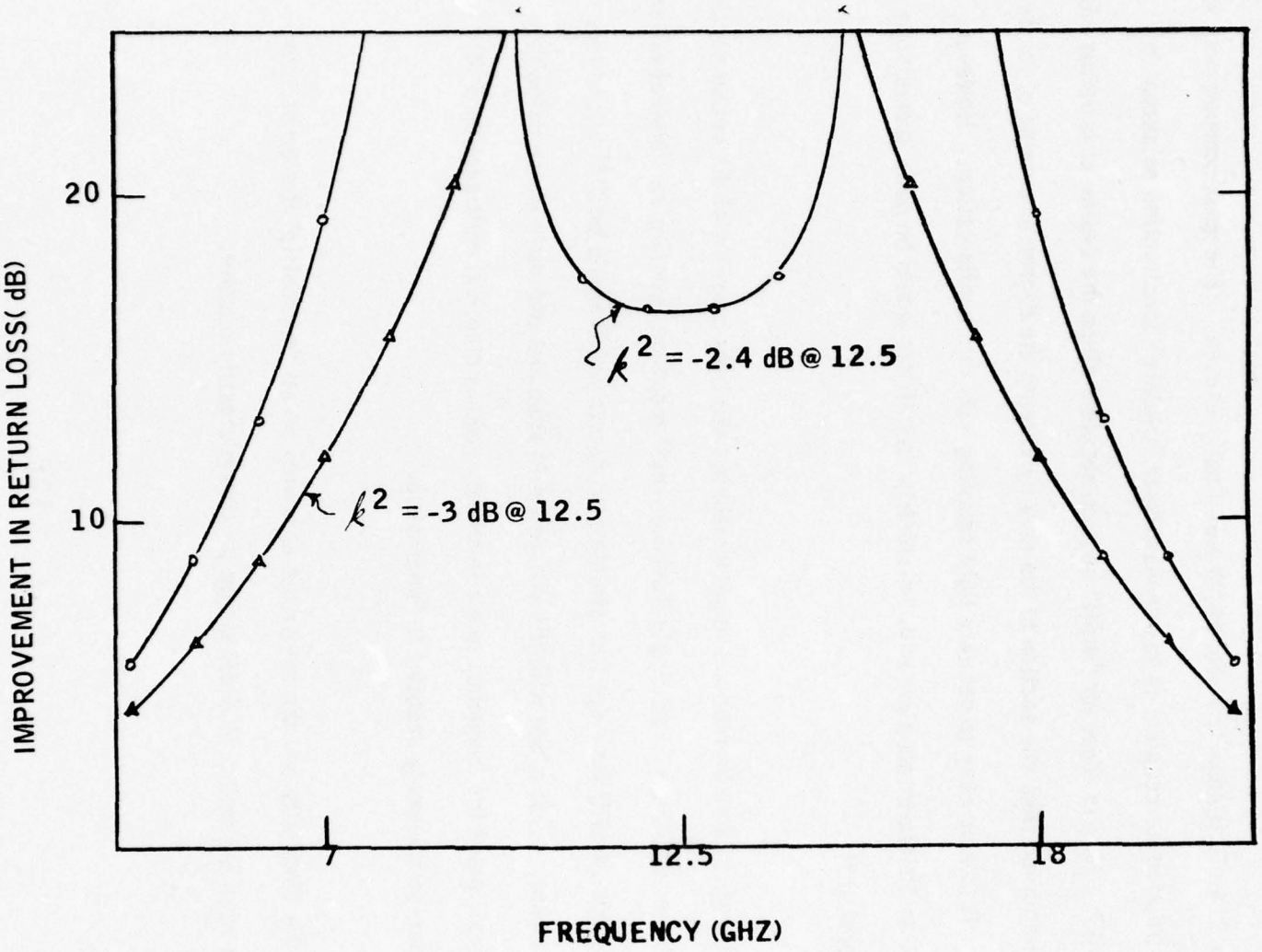
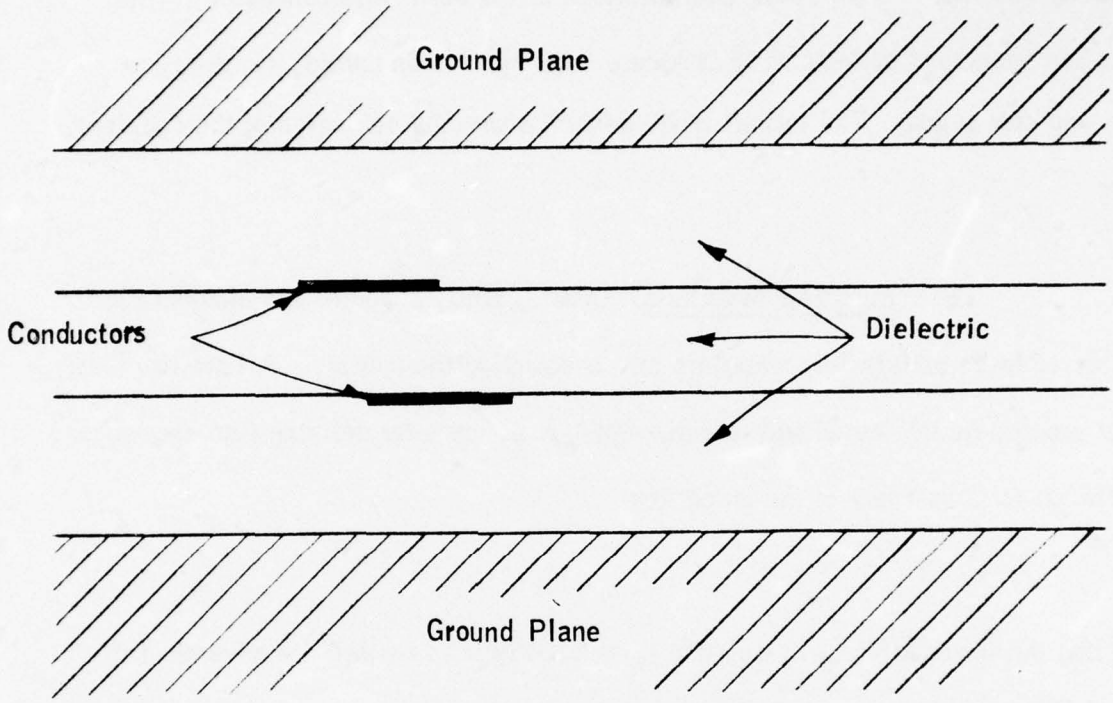

20
10
IMPROVEMENT IN RETURN LOSS(dB)
k^2 = -2.4 dB @ 12.5
k^2 = -3 dB @ 12.5
7
12.5
18
FREQUENCY (GHZ)

FIGURE 46

realization of a three section hybrid would be considerably more complicated than a one section 2.4 dB "Lange" coupler which was finally chosen. The most common method of construction for couplers is to use multilayer "triplate" construction as shown in Figure 47. This is ideal for "multi" section couplers since the degree of coupling can easily be varied from one section to the next by varying the degree of overlap of the two strips. It is also easy to get very tight coupling with this configuration. However, alternating "triplate" couplers with "microstrip" amplifiers would be quite cumbersome, and impractical.

A coupler could also be realized in microstrip but the tight coupling of the center section (1.5 dB for a 3 dB, -.3 dB ripple Tschebyscheff response) would give physical dimensions (about .4 Mil) for a six line structure on quartz which would be difficult to repeat in production. This along with the difference in even and odd mode phase velocities for microstrip and the frequency range involved, make a practical multisection 3 dB hybrid design extremely doubtful in "microstrip."

Thus, the simplicity and the advantage of having an all "microstrip" design dictated staying with an nominal 2.4 dB single section microstrip coupler.



Typical Tri Plate Construction of Couplers

Figure 47

2. Microstrip Interdigitated Quadrature

An interdigitated structure was first advocated by J. Lange[6] as a means of obta. tight coupling on "microstrip" with practical dimensions. The normal two conductors are broken up into four or more strips with alternate strips being interconnected. This technique has been used at Avantek to fabricate 3 dB hybrids on duroid, sapphire, alumina, and now quartz. The following are general comments on design of the couplers.

a. Substrate Materials: Quartz, BeO, sapphire and alumina were all considered to be satisfactory materials for constructing the hybrids. All are low loss materials and can be fabricated with surface finishes suitable for defining fine geometries. See Table XII for a summary of the properties.

Quartz has the lowest dielectric constant ($\varepsilon_r = 3.8$) which is a definite advantage in Ku-Band. At these frequencies dimensions have shrunk to the point where lower dielectric constant materials will give better tolerances in fabrication, better accuracy in converting calculated circuit elements into real dimensions and less problems in moding (conversion of energy into unwanted TE & TM modes). Unfortunately, the thermal conductance of Quartz is less than 1/20 that of sapphire and alumina, thus high dissipation semiconductors or resistors should not be mounted directly on a quartz substrate.

Parameter	Quartz	Sapphire	Alumina	Beo
ϵ_r	3.78	10	9.7 - 10	6.5
V/C_o (50 Ω Line)	.58	.40	.40	.47
Line Width/Substrate Height (50 Ω Line)	2.1	.95	.95	1.4
Length λ /4 @ 18 GHz (50 Line)	.095"	.066"	.066"	.077"
Loss Tangent	.0004	.0002	<.001	<.001
Thermal Conductivity (CA/S /CM/°C/SEC)	.0035	.08	.07	0.5
Thermal Expansion (1°C)	$.55X10^{-6}$	$8X10^{-6}$	$6X10^{-6}$	$7X10^{-6}$
Surface Finish	1-2μ"	1μ"	<4μ"	10μ"

TABLE XII

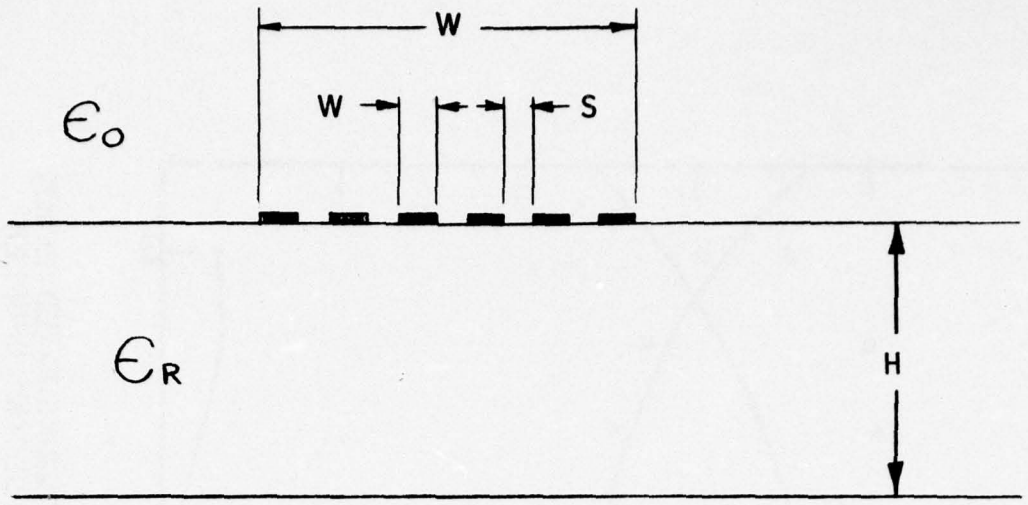
Substrate Materials

BeO would be a desirable substrate but Avantek is not presently set up to cut substrates internally. It is critical that RF grounds be located precisely at these frequencies either around the edge with small substrates or through holes.

Sapphire and alumina ceramic have essentially the same properties except that ceramic is much easier to cut and much less expensive. Either material would work satisfactorily provided that the substrate height was kept to 0.010" or less. The frequencies at which unwanted TE or TM waves begin to propagate is proportional to both substrate height and dielectric constant.

b. Design & Test Data: Two designs, one for 0.015" quartz and one for 0.025" alumina, are shown in Figure 48 and Table XIII. The substrate height was chosen to be as thin as possible and yet allow repeatable fabrication of line widths and separations. The criteria used was that the separation between lines be one mil or greater. It was planned, at first, to use quartz but metalization problems forced use of alumina for the 7-15 GHz amps.

However, quartz couplers were evaluated for the 7-18 GHz band with the following results. Figure 49 shows calculated and measured responses of the coupled and direct ports of a 2.4 dB hybrid. The figure also gives the coupler loss, calculated by adding the contributions from the coupled and direct arms and subtracting from unity.



Interdigitated Coupler Design
Figure 48

Coupler Characteristics, Quartz & Sapphire
Table XIII

Parameter	.015" Quartz	.025 Sapphire
f_o	12.5 GHz	11 GHz
k^2 (mid band coupling)	2.5 dB	2.5 dB
Z Odd	18.5	18.9
Z Even	134.9	132.3
Length -Even	.140"	.104"
Length-Odd	.152"	.114"
" of Strips	6	4
W/H	1.28	.45
W (Total Width)		
U (Strip Width)	.0020	.00190
S (Spacing)	.0014	.00115

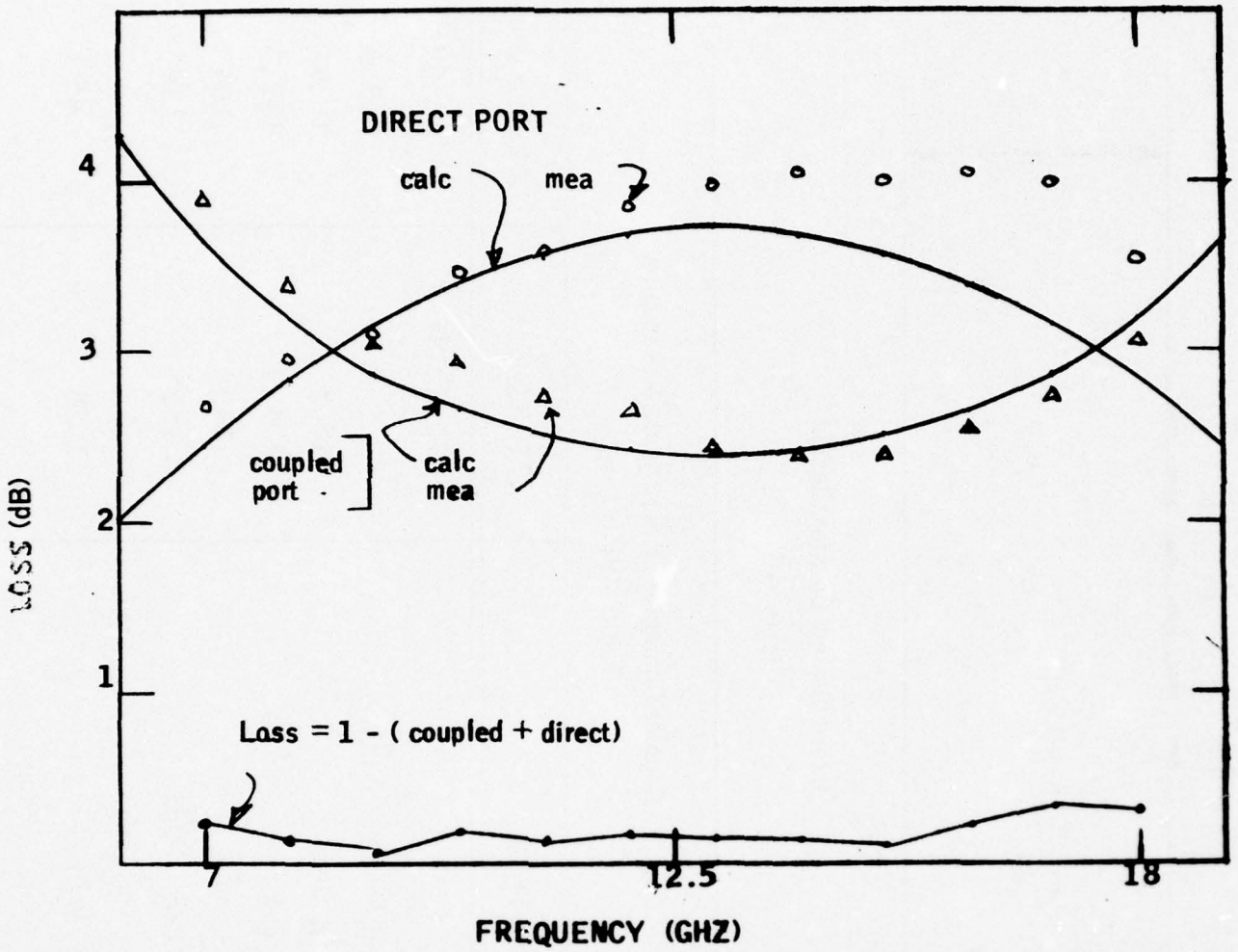


FIGURE 49 MEASURED PARAMETERS ON A 0.015" THICK INTERDIGITATED QUARTZ COUPLER. CALCULATED VALUES ARE FOR A 2.4 dB SINGLE SECTION COUPLER CENTERED AT 13 GHZ.

c. Fabricating Circuits on Quartz: Quartz is an extremely brittle material. When quartz is sawed, the edges are chipped and should be polished for small tolerances and smooth RF grounds. When quartz is scribed and broken, it does not always break along the scribed lines. However, when it does break where desired, the broken surface is smooth and the dimensions are precise.

Plating and etching quartz requires different techniques from plating and etching sapphire or alumina. Figure 50 shows coupler lines plated on quartz using our standard metal system for alumina. There was poor adhesion of the lines to the quartz which made ball-bonding impossible. Also, the lines were badly undercut by the etchant. The lower photograph, Figure 51, shows the latest results with a different metal system for plating the gold coupler lines. This system consists of a 500Å layer of tantalum, which is subsequently oxidized, followed by our normal metalization process. The oxidized layer of tantalum acts as a stress relief between the quartz and the overlying metalization. With this new metal system the adhesion is good, ball-bonding can be used, and there is very little, if any, undercutting. These photographs were taken with our scanning electron microscope. The coupler lines shown are about .002 inches wide.

3. Gain Versus Bandwidth Considerations

A simplified FET equivalent circuit and corresponding input and output matching circuits are shown in Figure 52. Using the data from Tables IX, X, and XI at 10 and 11 GHz, the values of R and C have been calculated for: (1) S_{11} and S_{22} match and (2) maximum available gain. For both cases, the Q of the input circuit is higher. Also, the Q of both circuits is higher for maximum available gain than they are for S_{11}

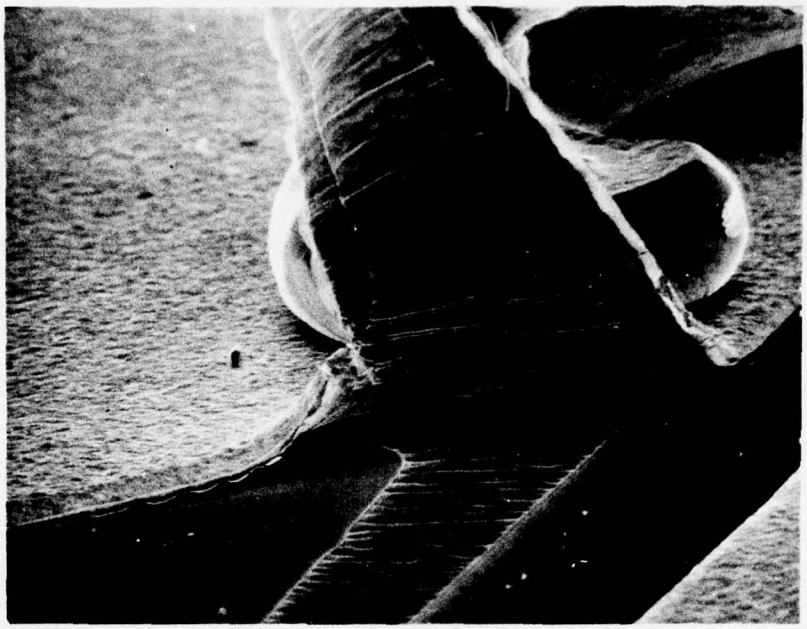


Figure 50. Plated gold on quartz metal system designed for alumina.

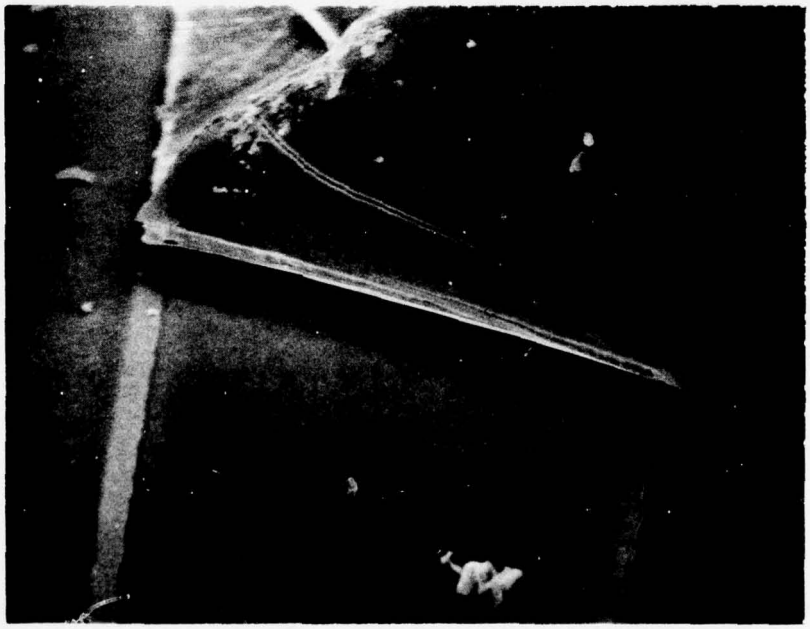
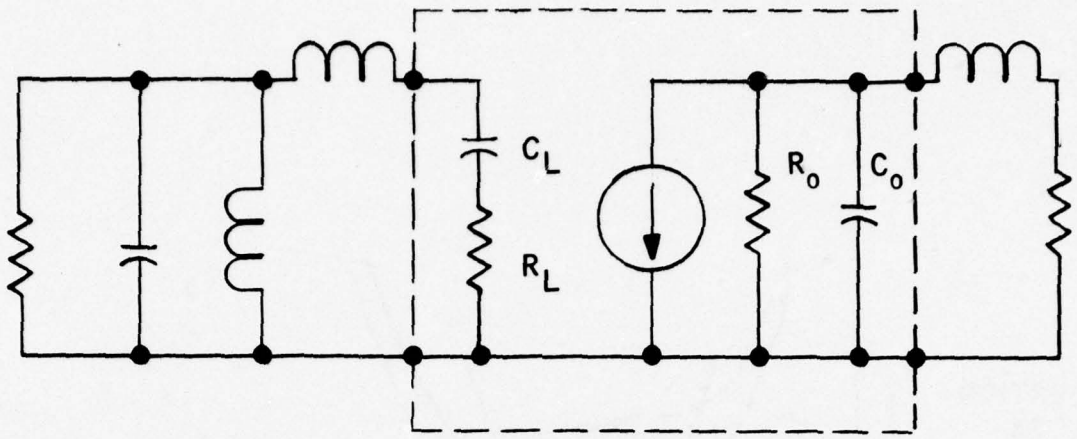


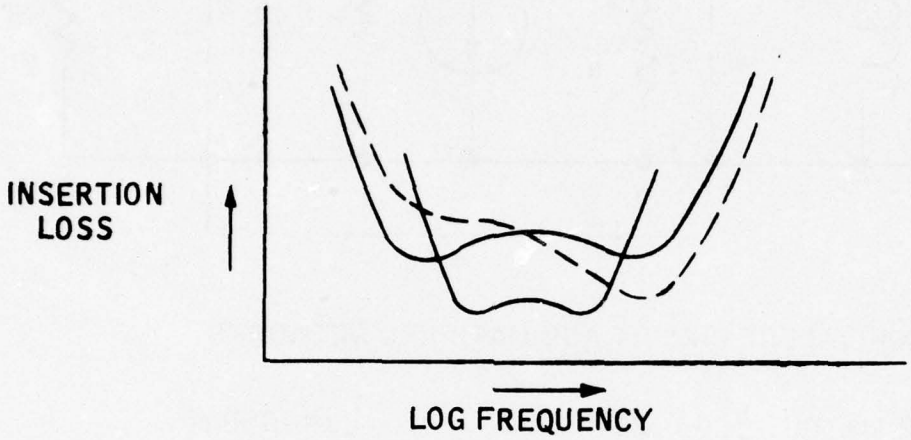
Figure 51. Plated gold on quartz metal system modified for quartz.



SIMPLIFIED EQUIVALENT CIRCUIT AND MATCHING NETWORKS

S PARAMETER MATCH	$C_L = 0.29$ pf	$Co = .058$ pf
	$R_L = 15$	$Ro = 200$
	$Q_L = \frac{1}{WoRC} = 3.74$	$Qo = WoRC = 0.76$
MAXIMUM AVAILABLE GAIN	$C_L = 0.25$ pf	$Co = 0.139$
	$R_L = 6.85$	$Ro = 345$
	$Q_L = 9.48$	$Qo = 3.16$

FIGURE 53



INSERTION LOSS OF INPUT MATCHING NETWORK

and S_{22} match. The insertion loss of the input circuit will be higher than the insertion loss of the output circuit, particularly if the circuits are adjusted for maximum available gain.

Considering the input and output separately and as loads, Fano's[7] equations show how the reflection coefficient or insertion loss is related to bandwidth and the RC product. For the input, series RC circuit, Fano's equation is:

$$\int_0^\infty \frac{1}{\omega^2} \ln \left| \frac{1}{p} \right| d\omega = \pi RC$$

Where p is the reflection coefficient at the input (also S_{11}).

A high value of RC, or low Q, will produce a low value of reflection coefficient and insertion loss.

For the output, parallel RC circuit, Fano's equation is:

$$\int_0^\infty \ln \left| \frac{1}{p} \right| d\omega = \frac{\pi}{RC}$$

A low value of RC, or low Q, will produce a low value of reflection coefficient and insertion loss.

Since the value of Q for the input circuit is higher than the Q of the output circuit, the insertion loss of the input circuit will be the highest for a given bandwidth. If Fano's equation for the input circuit is integrated, the insertion loss as a function of frequency is as shown in Figure 53. A narrow bandwidth corresponds to a low insertion loss and a wide bandwidth yields a higher insertion loss as indicated by the solid lines in the figure. If Fano's equation were integrated for a sloped response and a wide bandwidth, the dashed curve in Figure 53 would be obtained. It is seen that for the sloped response the insertion loss at the high frequency end of the band is much less than for the flat response.

The insertion loss of a matching network depends upon the number of elements in the network. The larger the number of elements, the smaller the insertion loss becomes until it reaches a minimum limit. In an actual FET circuit, maximum available gain will probably not be achieved, so that the Q of the input circuit will be less than the 9.48 shown in Figure 52. Assuming a Q of 7 and a 6 to 16 GHz frequency range, Figure 54 shows the minimum insertion loss of an infinite number of matching elements each having a constant insertion loss; and for elements which have an insertion loss that changes at 3 dB/octave. For comparison, the insertion loss for the input matching circuit ($n = 2$ for prototype network) in Figure 52 is shown. Both sloped responses have less loss at 15 GHz than the flat response for $n = \infty$. Also, the sloped insertion loss at 15 GHz could be reduced by .8 dB in $n = \infty$ instead of $n = 2$. If the slope had been greater than 3 dB/octave, the insertion loss at 15 GHz would have been reduced further.

INSERTION LOSS VERSUS NUMBER OF NETWORK ELEMENTS

Q = 7

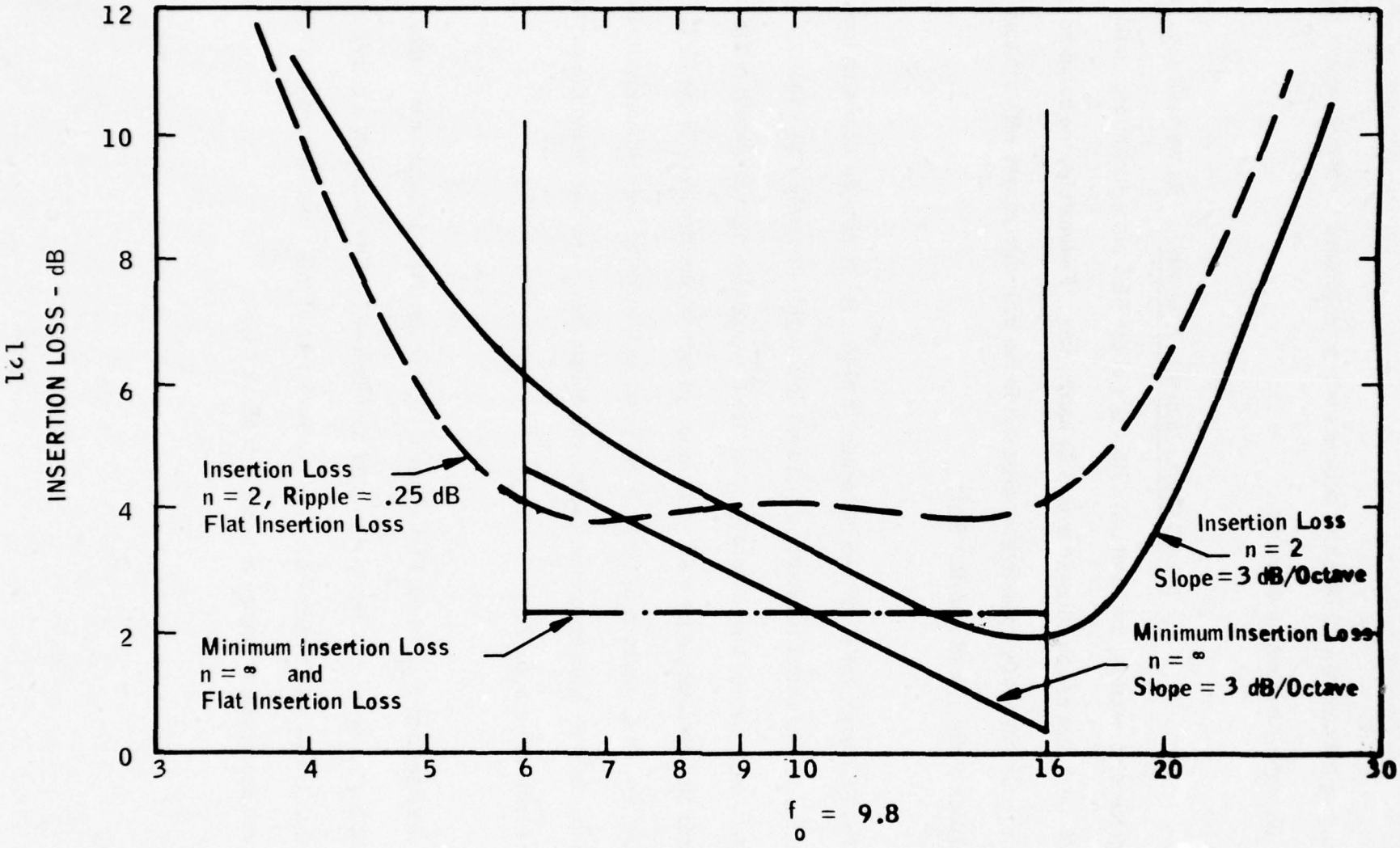


Figure 54

During the coming year matching networks will be developed for both input and output circuits with various numbers of elements.

a. Input & Output Matching Circuitry: As we have seen in the preceeding section, the input and output Q's of the FET place limitations on the degree of match that can be obtained over wide bandwidths. Fortunately, the balanced amplifier construction allows considerable mismatch in the individual stages with minimum degradation of the overall module VSWR.

The FET has a falloff of 5-6 dB/octave in MAG. By sloping the mismatch loss of both the input and output networks so that their loss varies inversely with frequency over the passband, we can simultaneously maximize the amount of gain bandwidth in the module and also compensate for the natural falloff in gain versus frequency of the FET. Since the highest Q occurs at the input of FET, we can maximize the gain bandwidth by making the input network have the greater slope in mismatch loss. The sum of the two mismatch losses is made to be 5-6 dB.

The measured S_{22} on the FET shows that a simple series inductance will rotate S_{22} on the Smith chart to nearly a matched condition at 15 GHz with only a couple of tenths of a dB loss (see Figure 41). The mismatch loss of this simple circuit increases monotonically with decreasing frequency to about 2.5 dB at 7 GHz.

The input matching circuit of the FET must have as low a mismatch loss at 15 GHz as possible to give high gain, and have about 4 dB additional loss at 7 GHz to produce a flat gain response. The initial networks were designed by trial and error. Potential networks were chosen by picking simple networks which on the Smith chart gave a match at 15 GHz. These circuits were then modeled on an Avantek C.A.D. program. An optimizing routine was then used to flatten and maximize gain over the 7-15 GHz bandwidth.

4. Single Stage Schematic and C.A.D. Results

Table XIV shows the calculated S-parameters for the optimized circuit, the input mismatch loss (MMLS 11), the output mismatch loss (MMLS 22), the transducer gain (TR 21), and the maximum available gain (MAG). The sum of the input and output loss plus the transducer gain approximately equals MAG. MAG is zero at 8 GHz and below because the device itself is unstable at these frequencies. The table also contains a schematic of the model used for the calculations.

Although the output network gives a monotonically increasing mismatch loss with decreasing frequency, the input network produces a double humped Tschebyscheff response. The peak to peak ripple can be adjusted by varying the input elements but flatness can only be obtained at the expense of gain. This was true not only for the computer calculations but also for the actual circuits. The ripple on each module was kept to less than ±.25 dB in order to meet the overall gain variation of ±1.5 dB. Figure 55 shows measured mesmatch loss, gain and MAG on a single ended developmental amplifier.

EVAL

TABLE XIV

F(GHZ)	SPAR 11	SPAR 11	SPAR 21	SPAR 21	SPAR 12	SPAR 12	SPAR 22	SPAR 22
4.000	0.99	17.57	2.11	-168.57	-27.32	122.43	0.82	45.58
6.000	0.91	-66.56	4.38	125.76	-21.89	69.06	0.73	15.70
7.000	0.87	-101.54	4.58	96.35	-20.49	46.35	0.67	2.77
8.000	0.82	-131.76	4.64	72.44	-19.78	30.04	0.61	-7.70
9.000	0.78	-158.07	4.44	48.91	-19.30	12.61	0.55	-18.77
10.000	0.74	176.24	4.34	28.34	-18.52	0.34	0.51	-26.64
11.000	0.71	153.00	4.31	4.34	-18.09	-12.90	0.45	-34.19
12.000	0.66	128.90	4.62	4.31	-17.29	-26.56	0.37	-43.64
13.000	0.64	104.74	4.54	4.62	-16.79	-39.20	0.31	-46.93
14.000	0.56	75.46	4.64	4.54	-16.00	-52.48	0.21	-51.95
15.000	0.53	38.20	4.17	4.64	-15.07	-69.04	0.10	-32.06
16.000	0.54	-8.34	1.12	4.17	-14.24	-93.69	0.19	49.01
18.000	0.61	-82.86		1.12	-15.58	-140.46	0.57	37.42

F(GHZ)	MMLS 11	MMLS 22	TR 21	MAG 0
4.000	-15.42	-4.75	2.11	0.00
6.000	-7.71	-3.36	4.38	0.00
7.000	-6.01	-2.54	4.58	0.00
8.000	-4.95	-2.05	4.64	0.00
9.000	-4.09	-1.58	4.46	10.34
10.000	-3.38	-1.29	4.44	9.09
11.000	-3.01	-0.97	4.34	8.18
12.000	-2.45	-0.65	4.31	7.30
13.000	-2.30	-0.44	4.62	7.26
14.000	-1.60	-0.19	4.54	6.31
15.000	-1.45	-0.04	4.64	6.19
16.000	-1.52	-0.17	4.17	6.04
18.000	-1.99	-1.70	1.12	5.31

** COMMAND

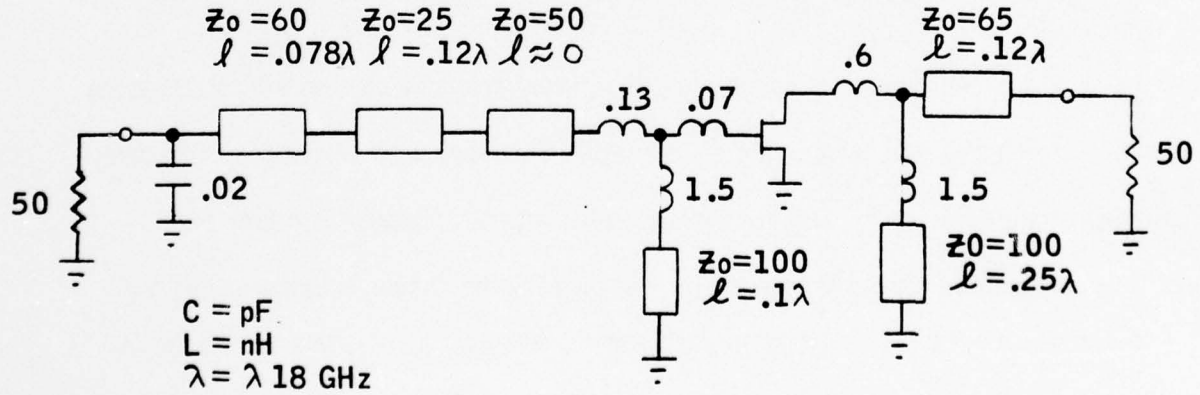
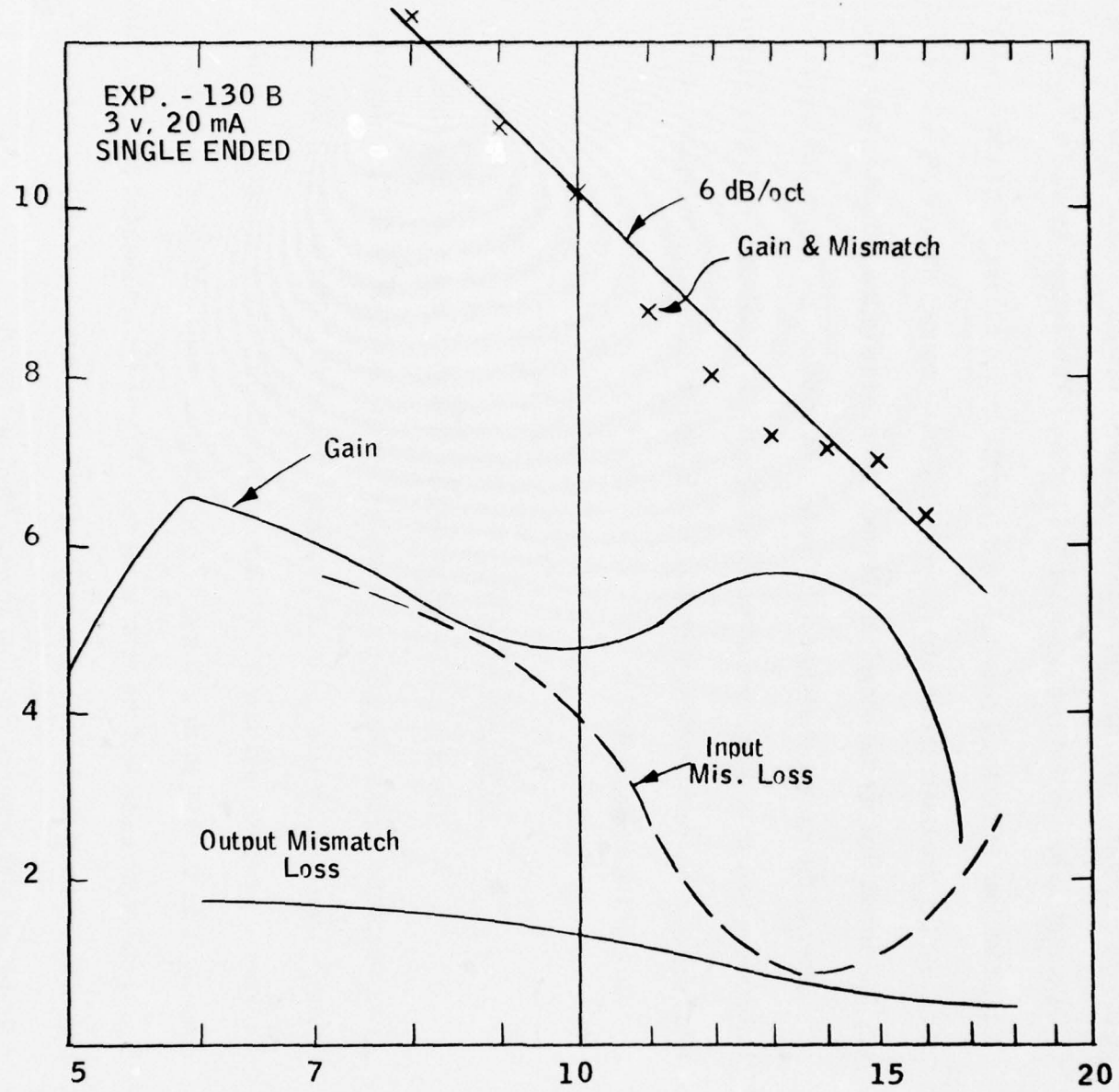


Figure 55, MEASURED MISMATCH LOSS, GAIN & MAG



Some difficulties were experienced in the earlier circuits with the 25 ohm section of line on the input circuit. This line was wide enough on the 0.025" thick alumina to cause some of the energy to be coupled into unwanted TM modes. This caused about 1 dB of additional dissipative loss in the input circuit. To reduce the losses caused by the undesired TM mode, the 25 ohm transmission line is cut up into small squares and rectangles. In this way the current flow for the undesired TM mode is forced to follow the same paths on the conductors as the current of desired TEM mode. In addition, the series and shunt inductances next to both gate and drain are smaller in the actual circuit. Better phase information in device characterization data should reduce the difference between the simulated and actual circuit.

5. Layout and Construction

The physical layout of the gain module is shown in Figure 56. There are five separate pieces which are soldered with Au Ge eutectic to a 0.015" thick Kovar carrier. Overall dimensions of the active circuit area are 0.300" wide by 0.245" long. The matching circuitry and coupler are fabricated on 0.025" thick alumina. The bias circuitry is on 0.010" thick alumina. RF and dc grounds are maintained by plating around one or more edges of the ceramic pieces. The FET's are mounted on top of a Kovar bar in the center of the circuit. The bar raises the FET to the level of the input and output circuitry and also provides isolation between input and output.

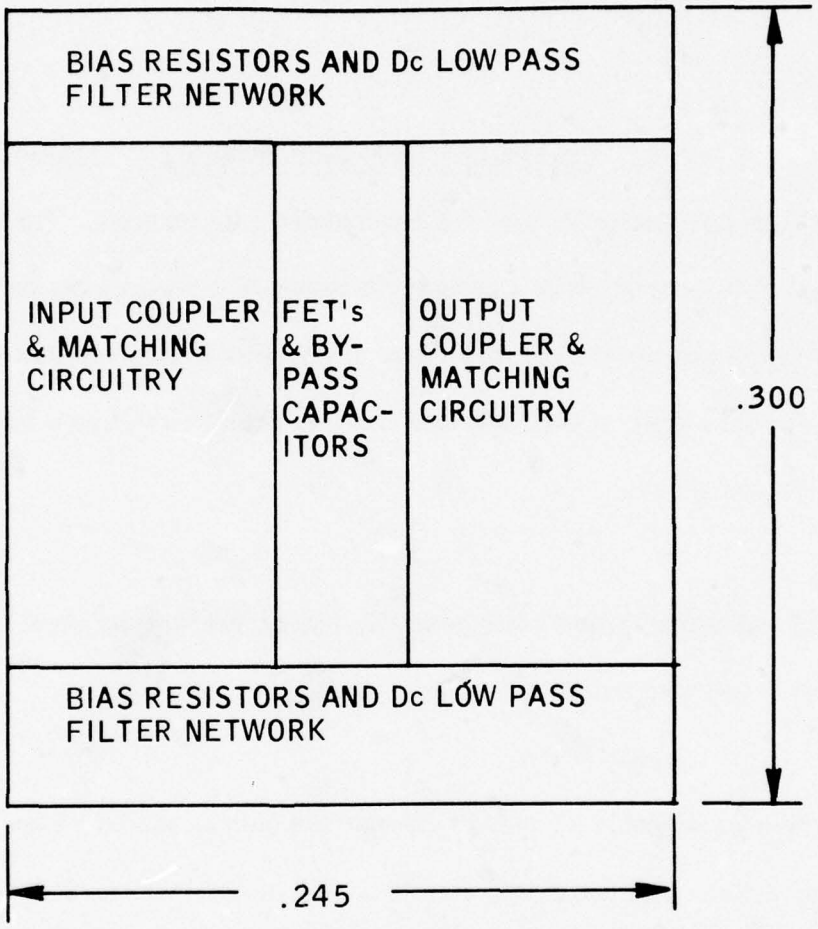


FIGURE 56 LAYOUT OF GAIN MODULE

6. Measured Results

a. Test Setup: Figure 57 is a photograph of our swept frequency test equipment. It is built around a Hewlett-Packard 86290A 2 to 18 GHz RF plug in 11667A power splitter, and Wiltron 501 logarithmic level meter, and 69A50 VSWR bridge.

b. Data on Individual Gain Modules: Table XV is an Automatic Network Analyzer listing for one of the completed gain modules. Table XIV is the simulated module listing from a computer program (without couplers or circuit losses). The gain shown on the two listings compare very well if an allowance of about .7 dB is made for the coupler and circuit losses. The actual circuit gain falls off more rapidly at 15 GHz and above.

The input and output VSWR's are generally low except that the input VSWR increases rapidly at 8 GHz and below.

One of the uses of Table XV was to compare the gain measured on our ANA and our swept-frequency setup. The two measurements agreed to within about 0.1 dB. Another use was to compare the absolute phase measured by the ANA for several gain modules. The ANA data indicated that the modules could be sorted into pairs with almost the same absolute phase across the 7 to 15 GHz frequency range. In addition, those gain modules with approximately the same absolute phase had a 1 dB gain change at the same frequencies

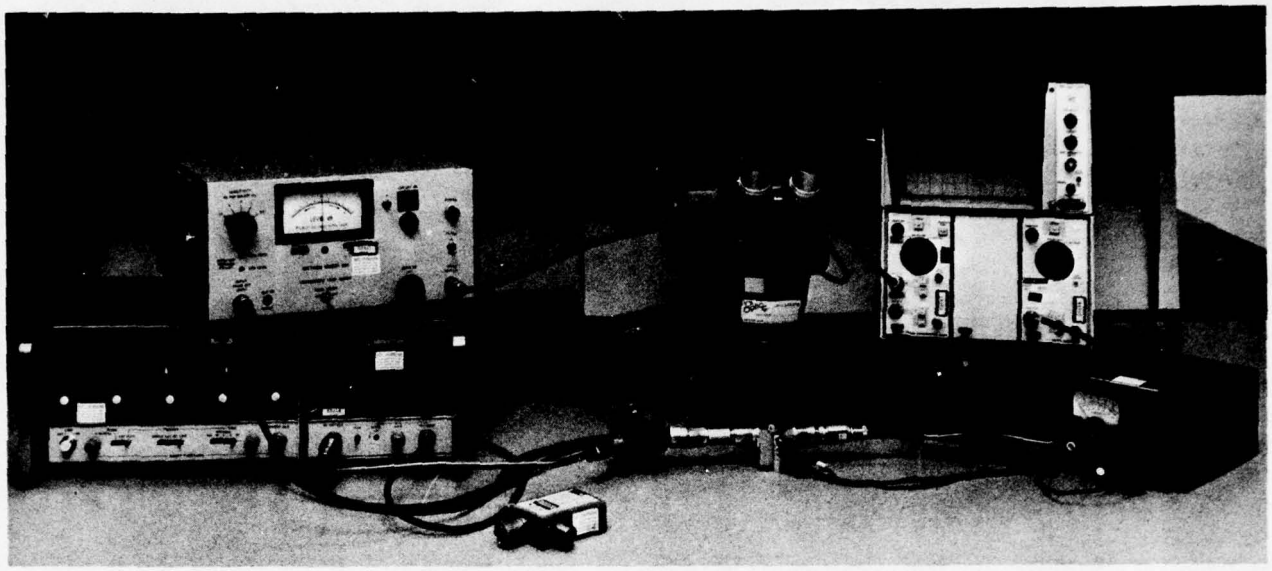


Figure 57

Swept Frequency Amplifier Test Equipment

MAY 19, 1976

Avantek inc.

7-15 GAIN MODULES
FET 150B
S/N 1A8 2A5

FREQ MHZ	VSWR IN	GAIN DB	PHASE DEG	PHASE DEV	FLAT DB	ISOL DB	VSWR OUT	FREQ MHZ
5000.0	2.80	2.39	-131.30			27.35	1.83	5000.0
5250.0	2.83	2.86	-141.83			26.65	1.74	5250.0
5500.0	2.84	3.16	-151.63			26.00	1.66	5500.0
5750.0	2.84	3.40	-161.97			25.29	1.58	5750.0
6000.0	2.79	3.56	-170.79			24.85	1.53	6000.0
6250.0	2.73	3.71	179.80			24.48	1.48	6250.0
6500.0	2.65	3.78	171.11			24.19	1.45	6500.0
6750.0	2.51	3.85	163.58			23.76	1.41	6750.0
7000.0	2.32	3.88	156.05	3.31	.00	23.73	1.39	7000.0
7250.0	2.16	3.94	148.84	2.12	-.06	23.45	1.37	7250.0
7500.0	2.03	4.00	142.15	1.44	-.12	23.26	1.37	7500.0
7750.0	1.90	4.05	135.24	.55	-.17	23.15	1.37	7750.0
8000.0	1.74	4.05	127.10	-1.56	-.18	23.06	1.36	8000.0
8250.0	1.62	3.98	120.04	-2.59	-.10	22.93	1.37	8250.0
8500.0	1.52	3.94	114.00	-2.62	-.06	22.97	1.37	8500.0
8750.0	1.44	3.82	108.90	-1.70	.04	22.86	1.37	8750.0
9000.0	1.38	3.85	102.77	-1.81	.02	22.74	1.38	9000.0
9250.0	1.35	3.83	96.57	-1.99	.04	22.67	1.39	9250.0
9500.0	1.34	3.84	89.69	-2.84	.03	22.55	1.40	9500.0
9750.0	1.34	3.63	84.19	-2.32	.23	22.51	1.40	9750.0
10000.0	1.35	3.77	79.06	-1.45	.10	22.38	1.41	10000.0
10250.0	1.38	3.69	73.81	-.67	.18	22.32	1.42	10250.0
10500.0	1.42	3.71	67.94	-.53	.16	22.21	1.42	10500.0
10750.0	1.44	3.67	62.86	.41	.20	22.12	1.41	10750.0
11000.0	1.47	3.72	57.59	1.14	.15	21.92	1.40	11000.0
11250.0	1.51	3.66	50.83	.39	.21	21.71	1.39	11250.0
11500.0	1.53	3.66	46.05	1.63	.21	21.70	1.38	11500.0
11750.0	1.56	3.73	40.27	1.85	.14	21.52	1.38	11750.0
12000.0	1.57	3.71	35.93	3.52	.16	21.49	1.36	12000.0
12250.0	1.58	4.03	29.67	3.28	-.15	21.01	1.36	12250.0
12500.0	1.58	3.95	23.27	2.90	-.07	21.07	1.35	12500.0
12750.0	1.56	3.99	16.23	1.88	-.11	20.83	1.36	12750.0
13000.0	1.54	3.87	11.07	2.75	.00	20.65	1.38	13000.0
13250.0	1.52	4.16	4.84	2.54	-.28	20.39	1.40	13250.0
13500.0	1.47	4.12	-2.05	1.67	-.24	20.23	1.42	13500.0
13750.0	1.44	4.07	-8.97	.77	-.19	20.01	1.46	13750.0
14000.0	1.39	4.01	-15.57	.19	-.13	19.80	1.49	14000.0
14250.0	1.32	4.09	-22.63	-.85	-.22	19.49	1.54	14250.0
14500.0	1.24	3.87	-30.04	-2.25	.00	19.47	1.58	14500.0
14750.0	1.16	3.86	-37.77	-3.97	.01	19.28	1.62	14750.0
15000.0	1.08	3.63	-45.01	-5.19	.24	19.26	1.65	15000.0
15250.0	1.04	3.37	-51.33			19.30	1.67	15250.0
15500.0	1.13	3.16	-60.35			19.26	1.68	15500.0
15750.0	1.25	2.83	-67.73			19.45	1.68	15750.0
16000.0	1.38	2.34	-75.87			19.70	1.67	16000.0
16250.0	1.51	1.99	-81.87			20.06	1.61	16250.0
16500.0	1.64	1.56	-89.63			20.26	1.60	16500.0
16750.0	1.72	1.01	-96.04			20.60	1.58	16750.0
17000.0	1.80	.47	-104.17			21.11	1.55	17000.0

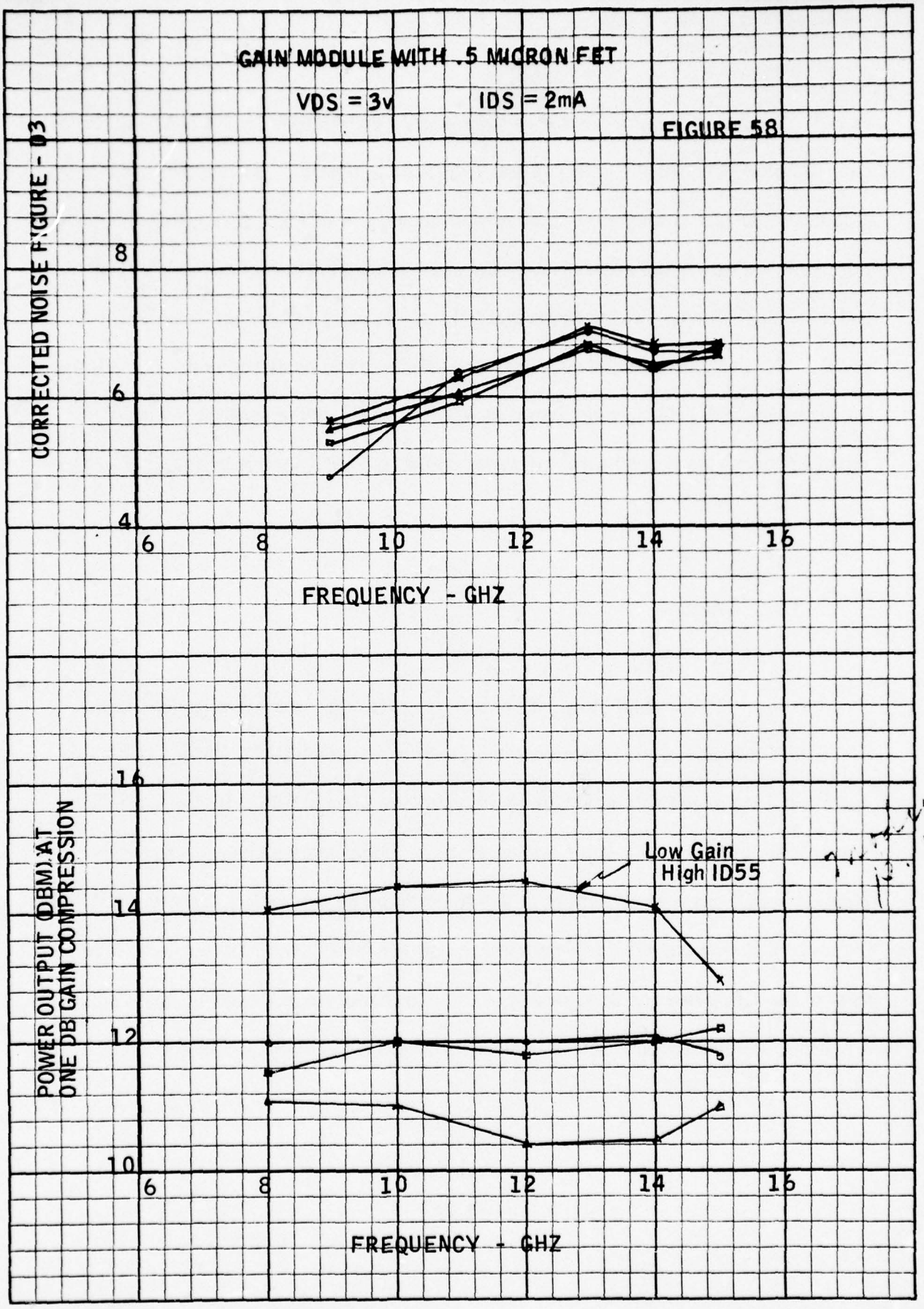
REF PLANES = 3.20 3.20 6.40

TABLE XV

GAIN MODULE WITH .5 MICRON FET

VDS = 3v IDS = 2mA

FIGURE 58

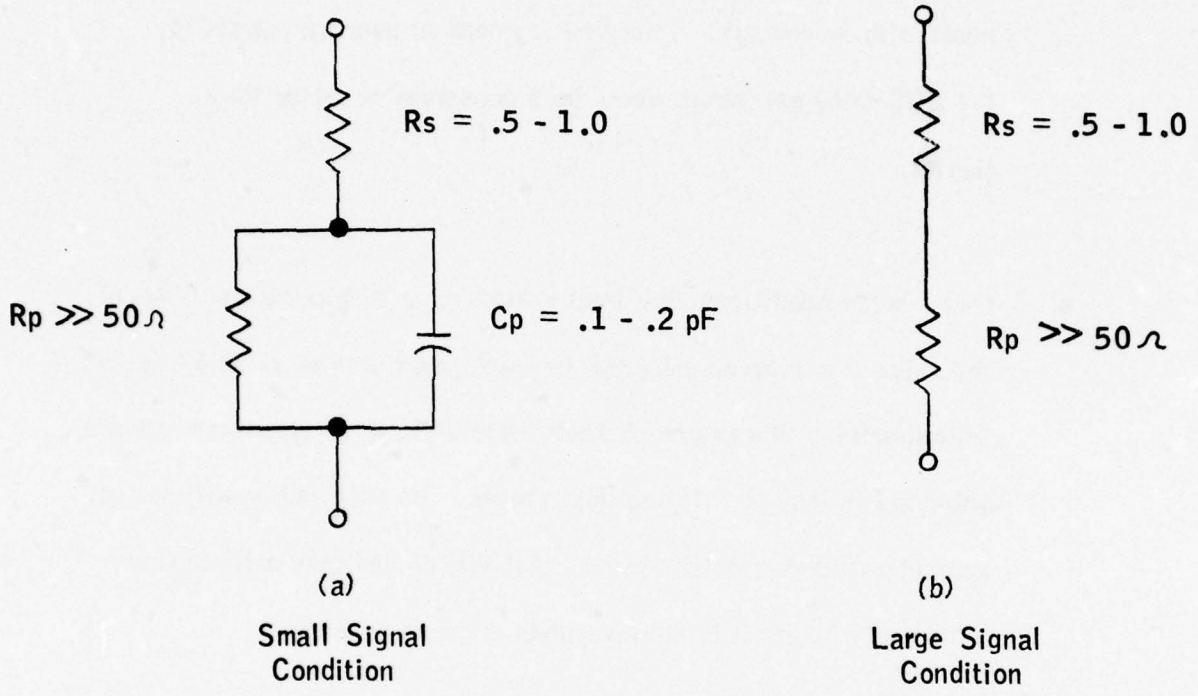


near the low and high band edges. In other words, the modules have a peak in their gain curves near 8 GHz and the gain is down 1 dB near 5.3 GHz. The modules also have a gain peak near 13.5 GHz and a 1 dB down frequency near 15.7 GHz. Pairs of modules were selected which had approximately the same shape gain curves at the band edges; and additional "tuning" was done so that gain curves were exactly the same at the band edges. The two gain modules were then put into the same positions in the two amplifiers. Noise figures and 1 dB gain compression were measured on the modules. Figure 58 shows the corrected noise figure and power output at 1 dB gain compression for several units.

C. Limiters

1. Theory

A solid state limiter utilizes PIN diodes in the following manner: The diodes are placed in shunt across the input transmission line. Under small signal conditions, the diode acts as a high impedance (see Figure 59) letting the RF signal pass through with a small amount of loss. Under large signal conditions the diode, either by rectifying a small amount of the signal or by an external dc current, fills its I region with charge and then acts as a very small r.f. resistance. In this state it reflects most of the r.f. power incident upon it and thus protects any components following it from r.f. damage either through thermal heating or excess r.f. voltage or currents.



Equivalent Circuit for a Pin Diode

Figure 59

A solid state diode limiter must thus have the following characteristics:

- It must limit r.f. leakage power to a level which will not damage the components which follow it. We have subjected balanced FET modules to CW power levels of up to 2 watts for periods of 24 hours with no damage. Thus limiting peak or average powers to the 200-500 mw range would be a conservative rating for a limiter.

- Under pulse conditions, the limiter must react within the rise time of the pulse if it is to be effective in protecting components which follow it. Unfortunately, this is one characteristic that limiter manufacturers are universal in leaving off their data sheets. No PIN limiter will protect against a "zero" rise time pulse. All PIN diodes take a finite time to turn on whether it is nano seconds or micro seconds.

- The limiter must be successful in protecting itself against high power, high duty cycle, and/or long pulse conditions.

2. Limiter Designs & Test Data

The following Table XVI describes the characteristics of three diodes that have been used in making various limiter configurations.

	BREAKDOWN VOLTAGE	CARRIER LIFETIME	RECTIFICATION EFFICIENCY	WILL WITHSTAND PEAK rf POWERS OF
VERY FAST LIMITING AND SWITCHING DIODES (PIN)	40-60V	10-15n sec	weak	100 watts
GENERAL PURPOSE DIODES (NIP)	200V	500n sec	none at all	500 watts
SCHOTTKY BARRIER DETECTOR DIODES	3-4 V		High	100 m watts

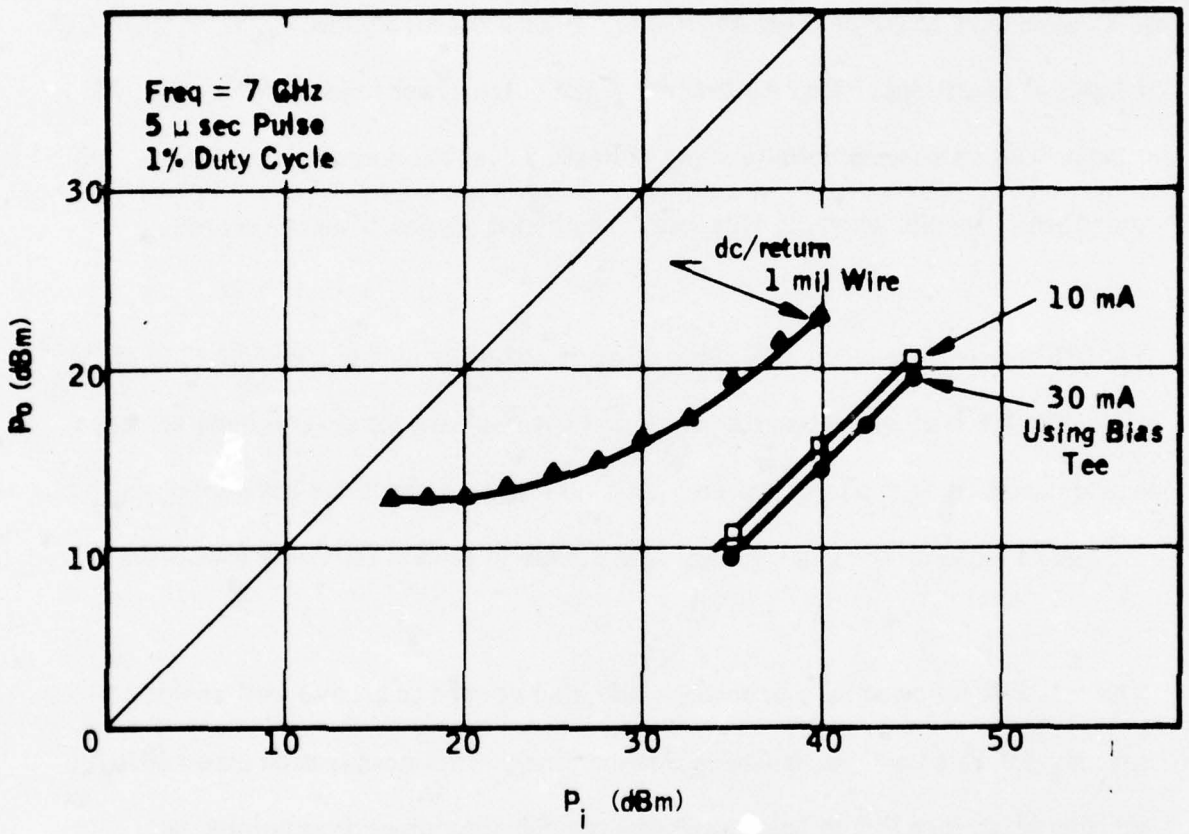
TABLE XVI

CHARACTERISTICS OF VARIOUS DIODES USED FOR MICROWAVE LIMITERS

The fast limiting diodes with lifetimes on the order of 10 nanoseconds rectify weakly above 7 GHz but do pass enough current to turn themselves on or to drive slower, higher current, PIN/NIP diodes. They do not, however, turn themselves on strongly enough to be effective for protection against long high power pulses (longer than 2 msec). Figure 60 gives the P_{in} versus P_{out} curve for one diode with a 1 mil gold wire as a dc return. The curve also shows the effects of driving the diode externally with both a 10 and 30 ma current source. With the ground return, the diode began to show drastic heating effects after 5 micro seconds of 10-20 watt pulses. A logical conclusion is that the device absorbs a much larger portion of the r.f. power (acts as a larger r.f. resistance) than when driven hard with an external dc current. The r.f. pulse showed no signs of the diode heating at the 40 watt level with 5 micro second pulses using external drive currents.

The general purpose diodes took a substantial fraction of a micro second to turn on but showed no signs of heating from long pulse lengths after being turned on. They had poor rectification efficiency above 7 GHz and had to be turned on externally either with a Schottky diode or a fast PIN. They also gave essentially no protection until they had been turned on.

The Schottky diodes had very high rectification efficiency and made very good drivers. However, if the diodes saw any portion of an r.f. pulse over 200 mw, they soon failed.



Limiting Data on One Fast PIN
Note Difference Between Using Rectified Current & External Bias

Figure 60

The following three two diode combinations were tested during the first part of the program. (See Figure 61) The only combination thought to be satisfactory at this stage was the two fast PIN diodes and a ground return (61a) with the provision that the pulse length be limited to 1μsec at 100 watts peak. Figure 62 shows measured loss and return loss on three of these limiters, two which were used in the delivery amplifiers. Figure 62 also gives P_{in} vs P_o both CW and pulsed conditions. Test equipment limited pulse power tests to 40 watts. All of these limiters showed definite signs of heating over the duration of the pulse with catastrophic results when the pulse was lengthened beyond 5 micro seconds.

The NIP followed by a fast PIN behaved much better for long pulse widths but the leakage on the leading edge of the pulse was about 1 watt for several hundred nano seconds until the NIP was turned on. This combination needs the addition of another fast PIN to clean up the leading edge of the pulse to protect following components.

The fast PIN followed by a Schottky diode also seemed to behave well at the 5 micro second, 40 watt level but isolation was marginal. This combination also needs the addition of another PIN in order to protect the Schottky diode from burning out.

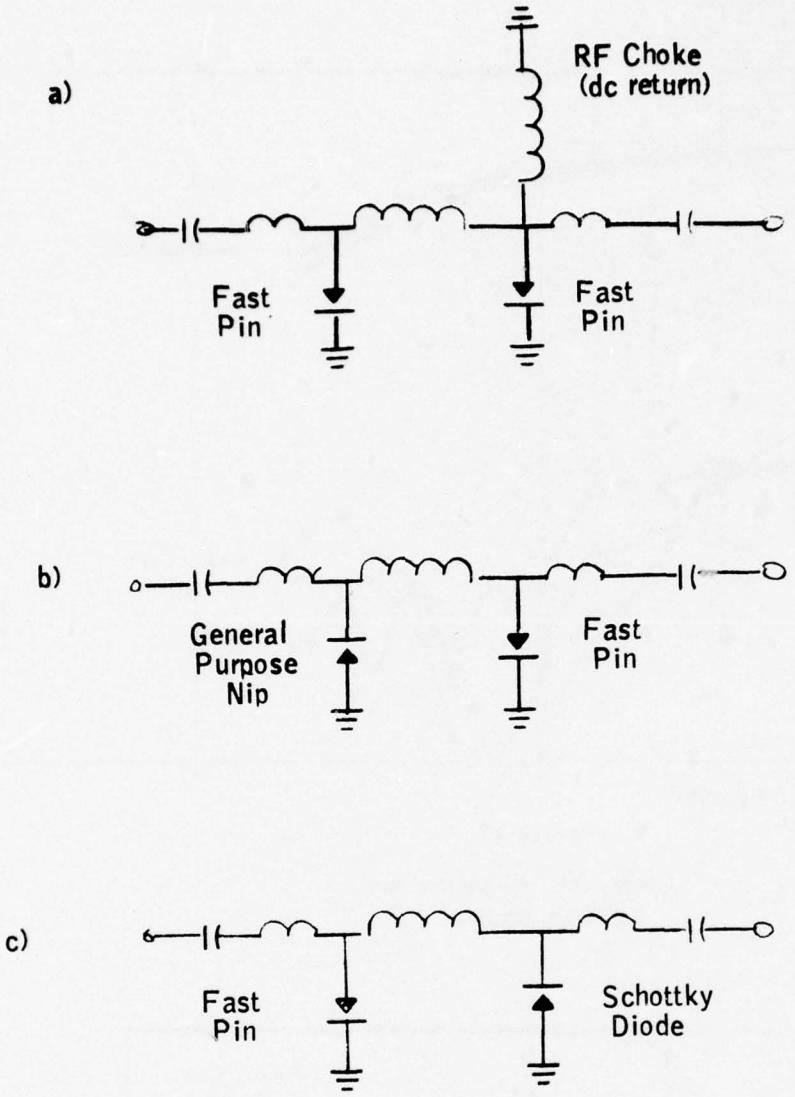


FIGURE 61. THREE TYPES OF TWO DIODE LIMITERS TESTED

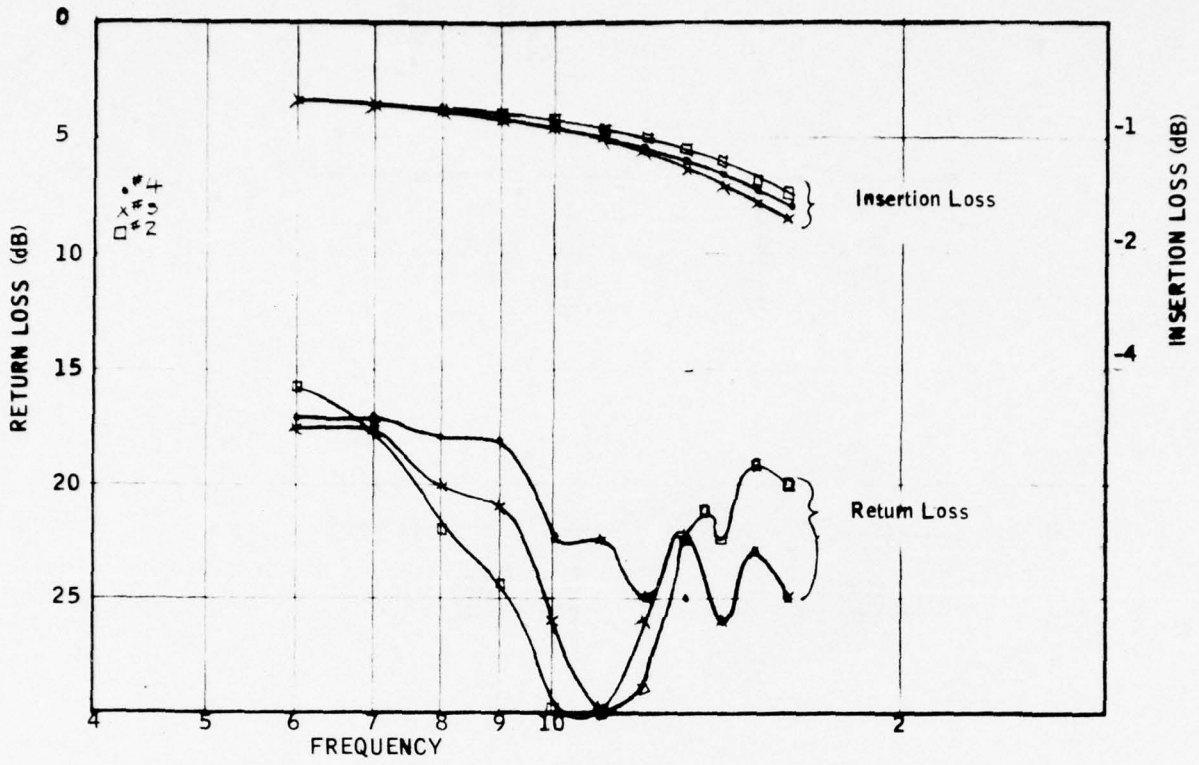


Figure 62

Return Loss and Insertion Loss
Delivery Limiters

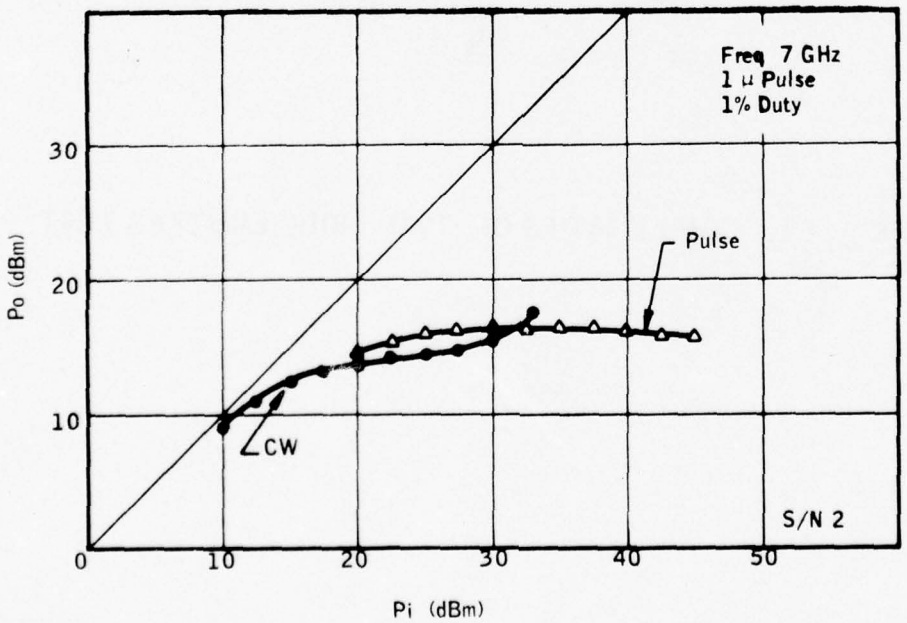


Table XVII summarizes the contract objectives for power handling capability, our proposed objectives, the results of the first half work, and objectives for the second half. It appears that in order to meet a 5 micro second, 100 watt peak pulse that the limiter will need at least three diodes. We have noted a considerable difference in loss among different diode lots. The loss can vary from as small as 0.3 - 0.4 dB, to as high as 0.8 dB per diode at 18 GHz. Therefore, the added pulse length capability could drastically effect the loss of the limiter under small signal conditions.

D. 7 to 15 GHz Amplifier

1. Block Diagram

Figure 63 shows a block diagram of the amplifier. At each end are right angle transitions from SMA connectors to microstrip. In the center is the eight volt regulator. If an external power supply is connected directly to the amplifier it must be able to supply 12 volts at approximately 400 mA.

The amplifier consists of a limiter followed by seven gain modules. Each gain module consists of a balanced amplifier with two FET's, an input, and an output coupler. Each module has a gain of approximately 4 dB.

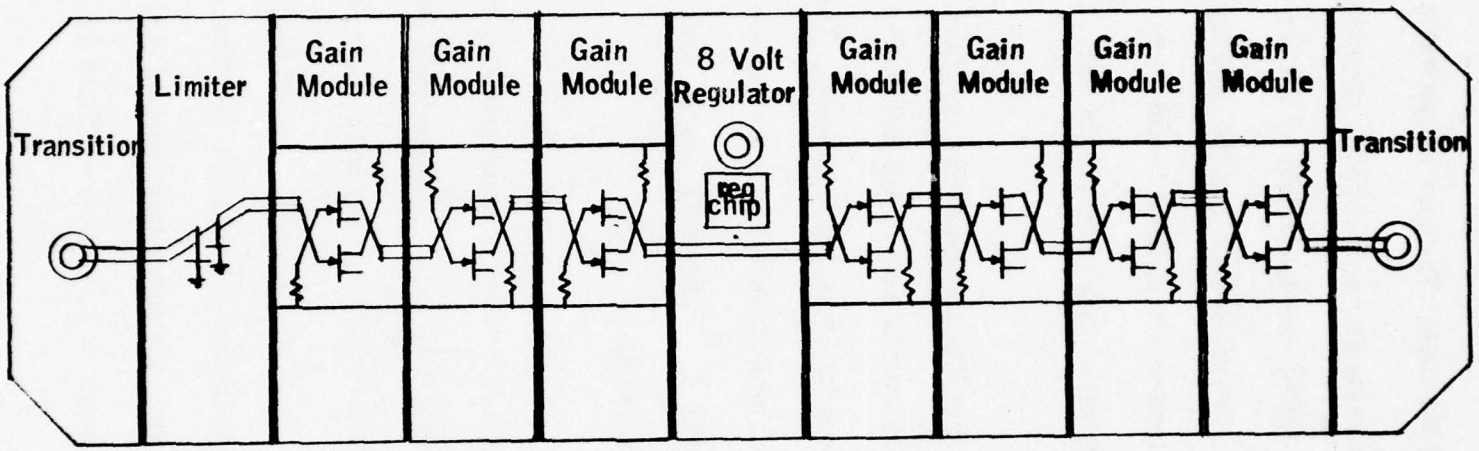
2. Case Design

The case which houses the amplifier is made of stainless steel. The components of the amplifier are mounted on 11 carriers as shown in Figure 63. These

	Statement of Work	Proposal	1st Half	Proposal for 2nd Half
CW Power	1 Watt	1 Watt	1 Watt	1 Watt
Pulse Condition Peak Power	100 Watts	100 Watts	100 Watts	100 Watts
Duty Cycle	10 %	1 %	1 %	1 %
Pulse Length	Undefined	1 μ sec	1 μ sec	5 μ sec
Rise Time	Undefined	Undefined	100 n sec	100 n sec
Frequency	7 - 15 7 - 18	———	7 - 15	7 - 18

Table XVII

Contract Objectives for Power Handling Capabilities



7 to 15 GHz AMPLIFIER

Figure 63

carriers are bolted to the top of the case. The case bottom has a milled slot which gives clearance for the carriers and components mounted on the case top. After the assembled amplifier has been adjusted and tested, the two halves of the case are welded together. Three glass feedthroughs are soldered into the case top. DC power to the 8 volt regulator is supplied through one of these feedthroughs. The other two feedthroughs are in the input and output coax transmission lines.

The RF transmission lines from the SMA connector thru the glass feedthroughs and right angle coax to microstrip transistions were tested with both a Time Delay Reflectometer (TDR) and the swept frequency test equipment. The TDR (with components to 12 GHz) was used for most tests since the cause of a particular reflection could be easily determined. Final tests thru 18 GHz were made with the swept frequency test equipment.

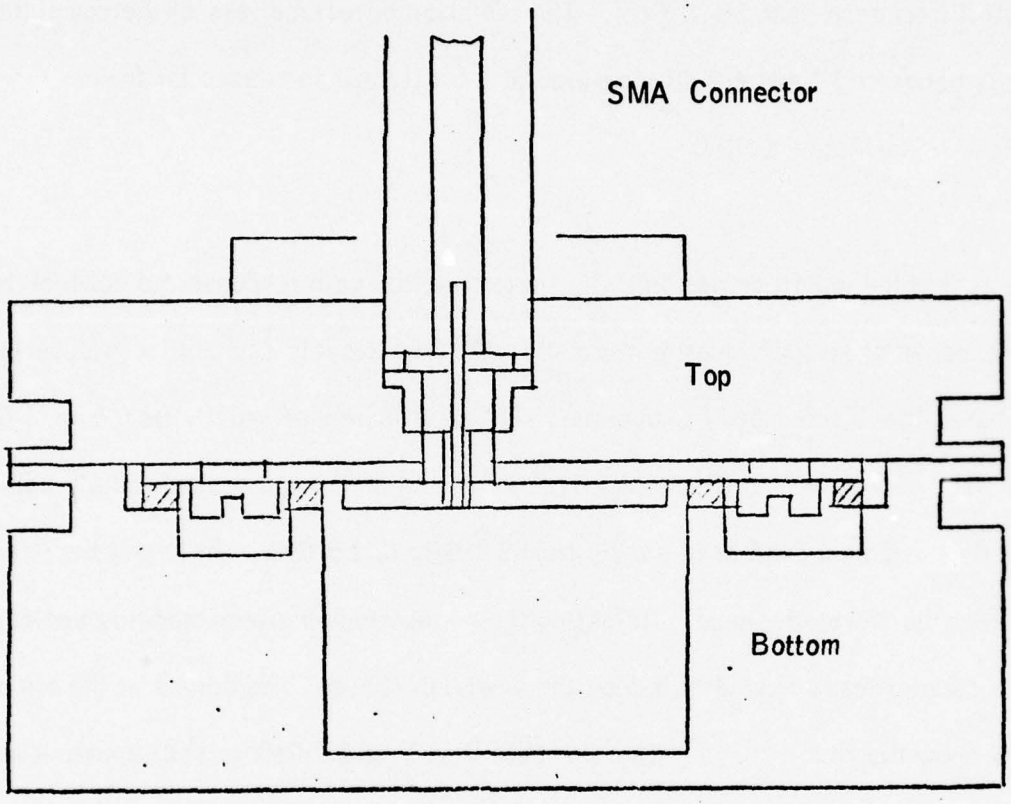
Microstrip loads with VSWR's of 1.11 or better were made with the 7mm coax to microstrip adapters shown in Figure 40. These loads were then mounted on carriers and placed next to the transition carriers on the case top. Looking into each SMA connector on the outside of case top, the effect of each discontinuity in the transmission lines was thus reduced to a low level. The final data on the RF transmission lines, looking into the SMA connectors, showed that the VSWR was less than 1.22 to 15 GHz with peaks to 1.4 between 15 and 18 GHz.

Figure 64 shows a cross section of the amplifier case. The slot in the case bottom extends from the input transition to the output transition. To prevent oscillation or distortion of the overall gain response, this slot was made a below-cutoff-waveguide with a cutoff frequency near 16.8 GHz. The isolation or reverse loss of the completed amplifier is between 50 and 60 dB measured at 16 GHz and increases for lower frequencies. (See Table XVIII).

When the assembled amplifier was initially turned on, the gain response did not look like the gain response of an individual gain module. A large 2 cycle sawtooth was superimposed upon the usual "double-humped" gain curve. The gain increased rapidly from 6 to 7 GHz and then decreased slowly from 7 GHz to nearly 10 GHz. The gain increased rapidly again from 10 to 12 GHz and then decreased slowly from 12 GHz to 15 GHz. Retuning the gain modules did not affect the sawtooth shape. Adjusting the connections between modules and capacitors across the coupler loads tended to reduce the sawtooth shape. The curves at the top of Figure 66 show the final results. The sawtooth from 7 to 10 GHz is still apparent and there are a couple of small bumps at higher frequencies. More effort is needed to understand and reduce these in-band gain variations and the corresponding phase changes.

3. Measured Data on Amplifier Without Limiter and Cables

Tables XVIII and XIX show data measured with the ANA on both amplifiers without limiters and without cables. The input VSWR has out-of-spec peaks near 7 and 12 GHz. The gain and gain flatness are within specs. The phase deviation



Cross Section of Ampifier Case

Figure 64

JUNE 1, 1976

7-15 GHZ GASFET AMPLIFIER
WITHOUT LIMITER
S/N 1

FREQ MHZ	VSWR IN	GAIN DB	FLAT DB	PHASE DEG	PHASE DEV	GPDEL NSEC	ISOL DB	VSWR OUT	FREQ MHZ
6000.0	2.35	25.92		-68.03		.00	87.06	1.44	6000.0
6250.0	2.39	28.42		157.28		1.49	84.82	1.40	6250.0
6500.0	2.41	30.07		23.64		1.47	91.62	1.39	6500.0
6750.0	2.34	31.15		-107.20		1.44	84.36	1.39	6750.0
7000.0	2.28	31.52	-1.49	124.21	27.30	1.40	78.89	1.38	7000.0
7250.0	2.12	31.12	-1.08	.35	10.74	1.34	88.47	1.38	7250.0
7500.0	1.92	30.69	-.06	-117.80	-.10	1.29	84.96	1.35	7500.0
7750.0	1.73	30.08	-.05	127.37	-7.62	1.25	90.31	1.31	7750.0
8000.0	1.59	29.42	.61	18.04	-9.63	1.21	83.97	1.26	8000.0
8250.0	1.46	29.34	.68	-90.81	-11.19	1.21	85.85	1.22	8250.0
8500.0	1.35	29.28	.74	160.81	-12.28	1.20	88.50	1.19	8500.0
8750.0	1.29	29.23	.79	52.94	-12.83	1.20	87.16	1.17	8750.0
9000.0	1.27	29.29	.73	-54.47	-12.94	1.19	91.40	1.16	9000.0
9250.0	1.27	29.23	.79	-162.04	-13.22	1.18	88.15	1.15	9250.0
9500.0	1.32	28.98	1.05	93.07	-10.80	1.16	86.88	1.15	9500.0
9750.0	1.39	28.93	1.09	-11.68	-8.26	1.16	94.83	1.15	9750.0
10000.0	1.50	28.91	1.11	-115.55	-4.81	1.15	86.58	1.17	10000.0
10250.0	1.63	28.96	1.06	142.13	.15	1.14	96.69	1.20	10250.0
10500.0	1.81	29.44	.58	38.86	4.19	1.16	87.95	1.25	10500.0
10750.0	1.95	29.86	.16	-66.50	6.11	1.17	93.63	1.31	10750.0
11000.0	2.13	30.13	-.10	-171.65	8.27	1.18	81.09	1.35	11000.0
11250.0	2.22	30.47	-.43	81.52	8.74	1.18	96.41	1.38	11250.0
11500.0	2.20	30.56	-.53	-24.89	9.64	1.18	84.15	1.40	11500.0
11750.0	2.06	30.71	-.68	-130.03	11.79	1.18	94.85	1.40	11750.0
12000.0	1.87	30.86	-.82	122.95	12.07	1.20	85.30	1.40	12000.0
12250.0	1.67	30.94	-.90	13.94	10.37	1.20	76.42	1.41	12250.0
12500.0	1.51	30.67	-.64	-92.83	10.90	1.20	79.03	1.34	12500.0
12750.0	1.39	30.73	-.70	158.70	9.73	1.20	89.56	1.33	12750.0
13000.0	1.33	30.59	-.56	51.61	9.94	1.20	90.62	1.33	13000.0
13250.0	1.32	30.54	-.51	-57.46	8.17	1.21	85.88	1.33	13250.0
13500.0	1.33	30.38	-.35	-166.79	6.15	1.22	78.53	1.32	13500.0
13750.0	1.34	30.21	-.18	83.13	3.37	1.21	90.48	1.36	13750.0
14000.0	1.36	29.91	.12	-25.18	2.36	1.22	86.68	1.40	14000.0
14250.0	1.35	29.95	.07	-136.50	-1.64	1.25	95.11	1.46	14250.0
14500.0	1.30	29.99	.03	109.80	-8.05	1.27	86.72	1.53	14500.0
14750.0	1.19	30.13	-.10	-5.56	-16.10	1.32	85.13	1.60	14750.0
15000.0	1.06	29.87	.15	-127.26	-30.50	1.38	83.04	1.60	15000.0
15250.0	1.10	29.07		106.75		1.39	83.27	1.52	15250.0
15500.0	1.17	26.87		-18.09		1.39	78.34	1.41	15500.0
15750.0	1.19	24.03		-142.79		1.35	65.11	1.35	15750.0
16000.0	1.21	20.24		99.08		.00	57.92	1.21	16000.0

LINEAR-IZATION RANGE	7000.0 TO 15000.0	7000.0 TO 15000.0

JUNE 1, 1976

TABLE XIX

Avantek inc.

7-15 GHZ GASFET AMPLIFIER
WITHOUT LIMITER
S/N 2

FREQ MHZ	VSWR IN	GAIN DB	FLAT DB	PHASE DEG	PHASE DEV	GPDEL NSEC	ISOL DB	VSWR OUT	FREQ MHZ
6000.0	1.55	25.24		-78.58		.00	82.21	1.65	6000.0
6250.0	1.67	27.80		146.84		1.49	87.47	1.60	6250.0
6500.0	1.81	29.45		12.71		1.48	84.25	1.56	6500.0
6750.0	1.96	30.19		-118.97		1.43	83.33	1.52	6750.0
7000.0	2.04	30.18	-1.34	115.34	28.54	1.37	83.18	1.47	7000.0
7250.0	2.05	29.89	-1.05	-5.01	15.18	1.32	86.70	1.42	7250.0
7500.0	2.07	29.73	-.89	-121.47	5.72	1.28	83.95	1.36	7500.0
7750.0	2.02	29.40	-.56	125.09	-.71	1.24	82.82	1.31	7750.0
8000.0	1.86	29.07	-.22	14.92	-3.89	1.22	89.74	1.24	8000.0
8250.0	1.63	29.30	-.46	-95.24	-7.05	1.23	93.14	1.20	8250.0
8500.0	1.43	29.39	-.55	154.15	-10.67	1.23	92.39	1.17	8500.0
8750.0	1.31	29.29	-.45	43.77	-14.05	1.22	89.15	1.16	8750.0
9000.0	1.27	29.18	-.34	-65.61	-16.44	1.21	82.90	1.16	9000.0
9250.0	1.26	28.83	.00	-174.22	-18.05	1.19	89.69	1.19	9250.0
9500.0	1.27	28.33	.50	80.52	-16.31	1.17	85.82	1.21	9500.0
9750.0	1.28	28.06	.77	-24.36	-14.20	1.16	90.33	1.24	9750.0
10000.0	1.32	27.83	1.00	-128.52	-11.36	1.15	82.16	1.27	10000.0
10250.0	1.34	27.56	1.27	129.08	-6.77	1.14	93.54	1.28	10250.0
10500.0	1.36	27.69	1.15	26.99	-1.87	1.14	86.14	1.27	10500.0
10750.0	1.37	27.94	.89	-76.43	1.69	1.15	93.86	1.25	10750.0
11000.0	1.47	28.13	.70	-179.77	5.34	1.16	90.72	1.21	11000.0
11250.0	1.64	28.55	.28	75.10	7.20	1.18	81.45	1.19	11250.0
11500.0	1.83	28.69	.14	-31.39	7.70	1.17	93.10	1.19	11500.0
11750.0	1.98	28.72	.11	-136.00	10.09	1.17	80.90	1.19	11750.0
12000.0	2.01	28.74	.10	117.74	10.83	1.19	86.79	1.20	12000.0
12250.0	1.95	28.80	.03	10.35	10.42	1.18	76.16	1.21	12250.0
12500.0	1.85	28.56	.27	-94.03	13.04	1.17	83.44	1.17	12500.0
12750.0	1.73	28.66	.17	159.09	13.16	1.19	90.97	1.16	12750.0
13000.0	1.65	28.72	.11	52.14	13.20	1.19	85.46	1.18	13000.0
13250.0	1.60	28.79	.04	-55.48	12.57	1.20	88.22	1.22	13250.0
13500.0	1.60	28.83	.00	-163.45	11.61	1.21	87.62	1.31	13500.0
13750.0	1.58	28.98	-.14	86.14	8.19	1.22	86.50	1.44	13750.0
14000.0	1.50	28.99	-.15	-22.89	6.15	1.23	82.70	1.59	14000.0
14250.0	1.38	29.26	-.42	-136.04	.00	1.27	100.21	1.71	14250.0
14500.0	1.25	29.33	-.48	109.19	-7.77	1.29	86.89	1.82	14500.0
14750.0	1.15	29.35	-.51	-8.38	-18.34	1.33	82.37	1.87	14750.0
15000.0	1.10	28.84	.00	-130.18	-33.15	1.37	81.12	1.81	15000.0
15250.0	1.16	27.91		104.40		1.39	79.86	1.71	15250.0
15500.0	1.26	25.79		-20.05		1.37	77.96	1.63	15500.0
15750.0	1.32	23.20		-141.79		1.36	69.39	1.63	15750.0
16000.0	1.32	20.51		95.28		.00	59.52	1.53	16000.0

LINEARIZATION RANGE	7000.0 TO 15000.0	7000.0 TO 15000.0

is within ±15° from 7.5 to 14.50 GHz, but there are peaks of nearly 30° at 7 and at 15 GHz. To reduce the phase deviation further will require broader band amplifiers with less ripple.

The isolation measurement, in general, indicates the noise level of the ANA. The isolation shown at 15.75 and 16 GHz shows the loss in the below-cutoff waveguide formed between the top and bottom of the amplifier case.

Figure 65 shows the measured amplifier noise figure and power output at 1 dB gain compression without limiters and without cables. The noise figure for S/N 2 is almost 1 dB greater than the noise figure of S/N 1 at 12 GHz. Yet, the first gain modules in each amplifier had similar corrected noise figures. The first gain module in amplifier, S/N 2, had more gain than the first module in S/N 1.

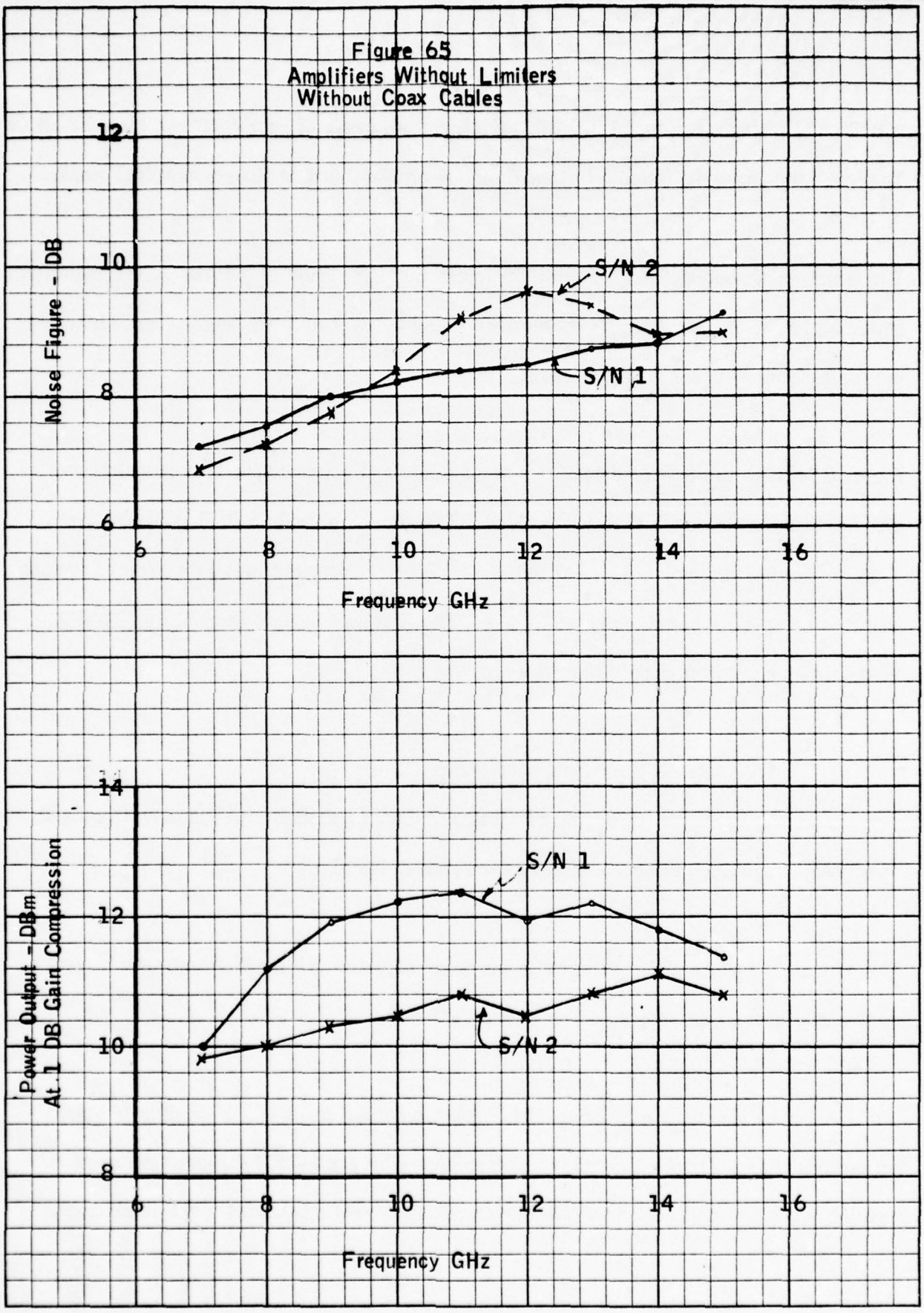
4. Phase Matching Considerations

Table XX shows a listing of the gain and phase for both amplifiers and the difference between the gains (DG 12) and phases (DP 12).

The individual modules were selected in pairs and adjusted to have the same gain curves, particularly at the band edges. (See Section V 36B)

Each assembled amplifier was adjusted to have a response as close as possible to a double-hump rather than a 2-cycle sawtooth. The problem with achieving this goal appears to stem from the interstage connections or discontinuities (see Section V, D2). The interstage

Figure 65
Amplifiers Without Limiters
Without Coax Cables



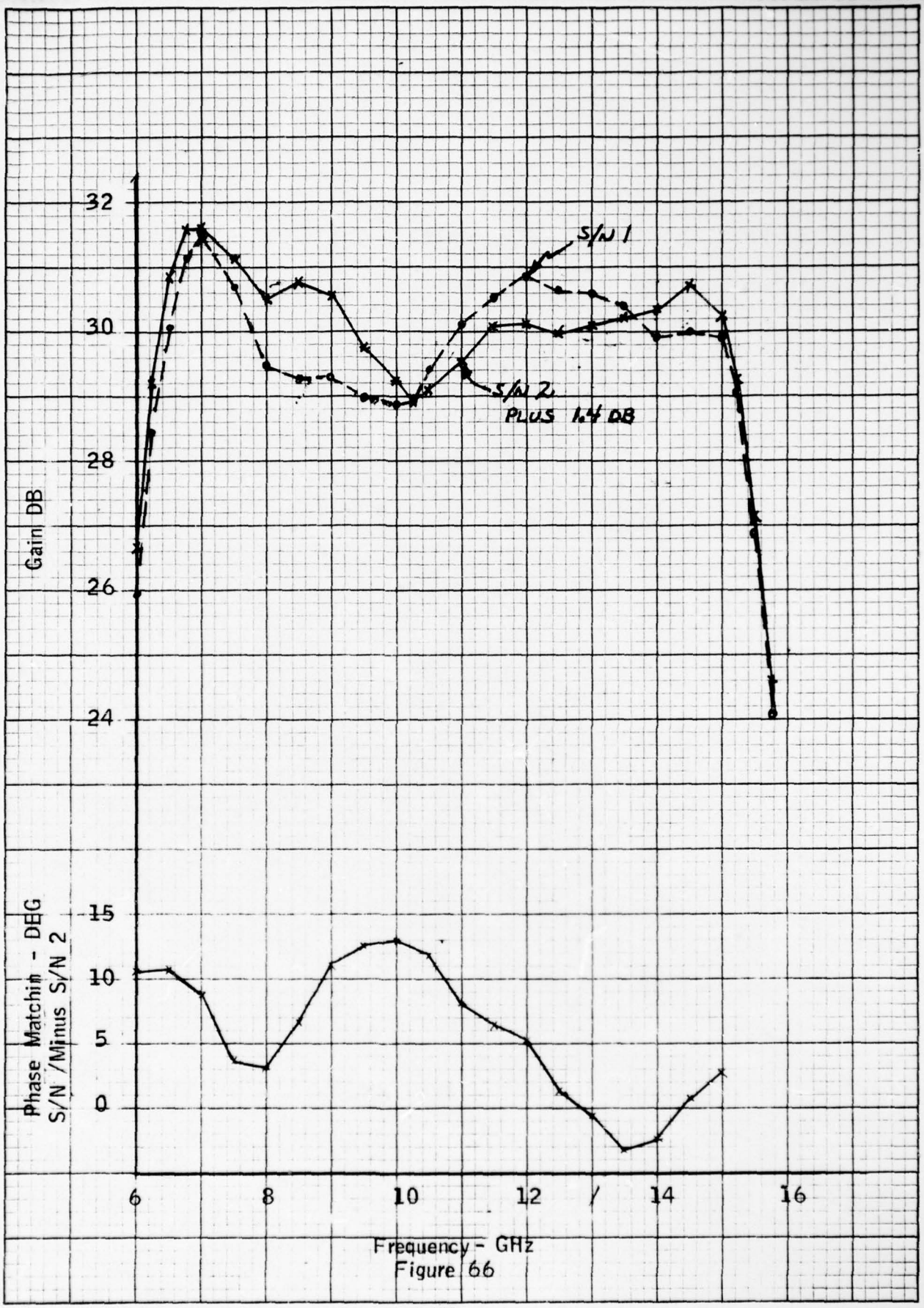

32
30
28
26
24
Gain DB
S/N 1
S/N 2
PLUS 1.4 DB
15
10
5
0
Phase Matchin - DEG
S/N /Minus S/N 2
6
8
10
12
14
16
Frequency - GHz

Figure 66

JUNE 1, 1976

7-15 GHZ GASFET AMPLIFIER
WITHOUT LIMITER

S21 IN DB

FREQ	S/N 1 GAIN	PHASE	DG12	DP12	S/N 2 GAIN	PHASE
7000.0	31.52	124.2	1.35	8.9	30.18	115.3
7250.0	31.12	.3	1.23	5.4	29.89	-5.0
7500.0	30.69	-117.8	.96	3.7	29.73	-121.5
7750.0	30.08	127.4	.68	2.3	29.40	125.1
8000.0	29.42	18.0	.35	3.1	29.07	14.9
8250.0	29.34	-90.8	.04	4.4	29.30	-95.2
8500.0	29.28	160.8	-.11	6.7	29.39	154.1
8750.0	29.23	52.9	-.06	9.2	29.29	43.8
9000.0	29.29	-54.5	.12	11.1	29.18	-65.6
9250.0	29.23	-162.0	.40	12.2	28.83	-174.2
9500.0	28.98	93.1	.65	12.6	28.33	80.5
9750.0	28.93	-11.7	.87	12.7	28.06	-24.4
10000.	28.91	-115.5	1.08	13.0	27.83	-128.5
10250.	28.96	142.1	1.40	13.1	27.56	129.1
10500.	29.44	38.9	1.76	11.9	27.69	27.0
10750.	29.86	-66.5	1.92	9.9	27.94	-76.4
11000.	30.13	-171.6	2.01	8.1	28.13	-179.8
0.	30.47	81.5	1.92	6.4	28.55	75.1
0.	30.56	-24.9	1.87	6.5	28.69	-31.4
11750.	30.71	-130.0	1.99	6.0	28.72	-136.0
12000.	30.86	122.9	2.12	5.2	28.74	117.7
12250.	30.94	13.9	2.14	3.6	28.80	10.3
12500.	30.67	-92.8	2.11	1.2	28.56	-94.0
12750.	30.73	158.7	2.07	-.4	28.66	159.1
13000.	30.59	51.6	1.87	-.5	28.72	52.1
13250.	30.54	-57.5	1.75	-2.0	28.79	-55.5
13500.	30.38	-166.8	1.55	-3.3	28.83	-163.4
13750.	30.21	83.1	1.23	-3.0	28.98	86.1
14000.	29.91	-25.2	.91	-2.3	28.99	-22.9
14250.	29.95	-136.5	.69	-.5	29.26	-136.0
14500.	29.99	109.8	.67	.6	29.33	109.2
14750.	30.13	-5.6	.78	2.8	29.35	-8.4
15000.	29.87	-127.3	1.03	2.9	28.84	-130.2

TABLE XX

discontinuities, at frequencies where their effects reinforce each other, mask the final gain shape until the amplifier is completely assembled.

Figure 66 compares the gain of one amplifier (S/N 1) to the gain of the other amplifier (S/N 2 plus 1.4 dB) as might be seen on the swept frequency test equipment. At the bottom of the page the phase tracking between the two amplifiers is shown. At 7 GHz, S/N 2 is electrically longer than S/N 1 since its absolute phase angle has rotated farther (see Tables XVIII and XIX). From 7 to 8 GHz and from 10.25 to 12 GHz, S/N 1 has a greater gain slope magnitude and is electrically longer than S/N 2 as indicated by their group delays (GPDEL). Similarly, S/N 2 has a greater gain slope between 8.5 and 9.5 and between 14 and 15 GHz and has a larger group delay between these frequencies. Comparing gain slope with phase matching, it is seen that when S/N 1 is longer, the matching error tends toward zero as from 7 to 8 GHz and again from 10.25 to 12 GHz.

5. Amplifiers with Limiters

Tables XXI - XXIII and Figure 67 show data on the amplifiers after adding the limiters. Limiter data is shown in Figure 62. The effect of the limiters did not seem to be always the same. The peak in the input VSWR near 12 GHz was removed for both S/N 1 and S/N 2. However, the loss did not add equally to the noise figure of each amplifier. In fact, the net effect was to cause the noise figure of each amplifier to be

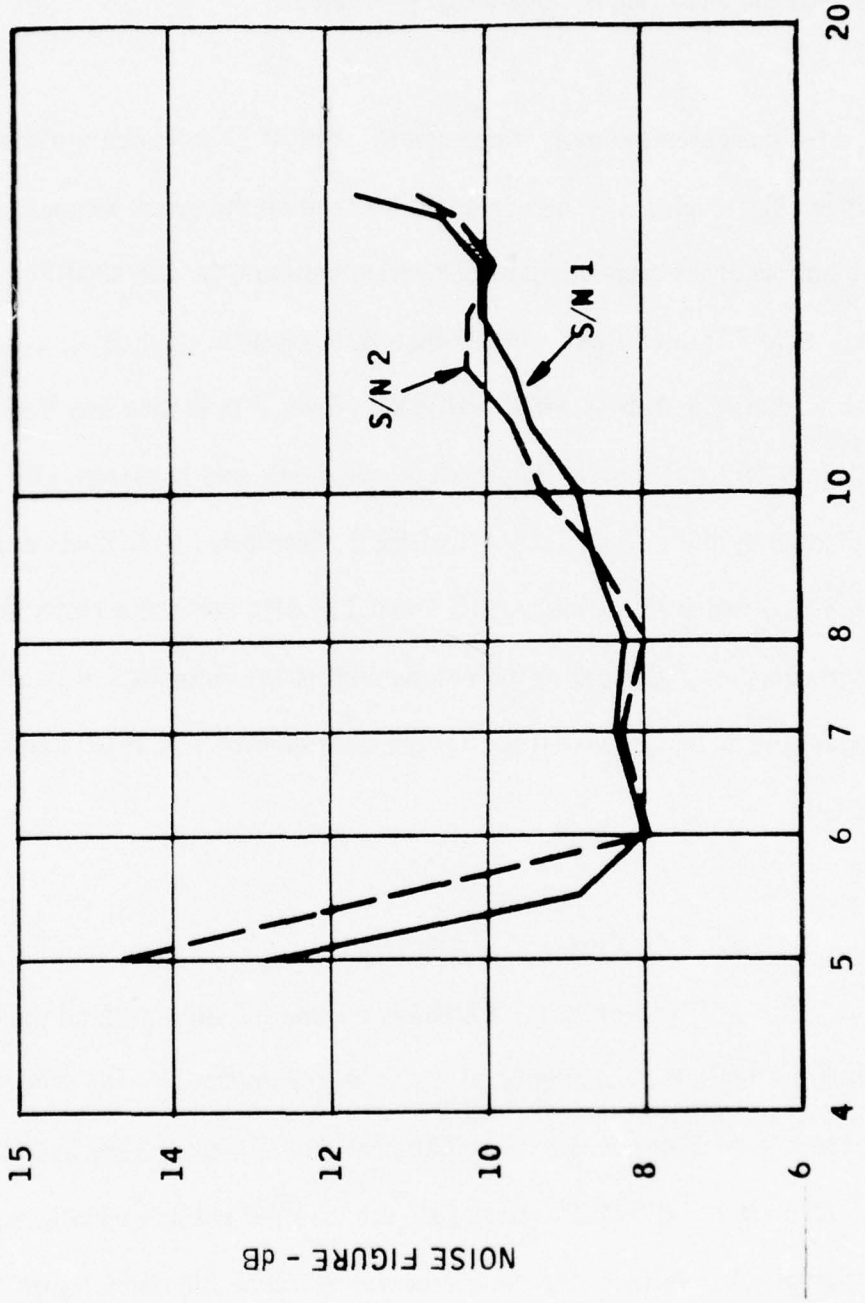


Figure 67
NOISE FIGURE
AMPLIFIERS WITH LIMITERS
WITHOUT CABLES

JUNE 3, 1976

7-15 GASFET AMPLIFIER

S/N 1

FREQ MHZ	VSWR IN	GAIN DB	FLAT DB	PHASE DEG	PHASE DEV	GPDEL NSEC	ISOL DB	VSWR OUT
6000.0	1.91	24.98		-81.60		.00	88.34	1.39
6250.0	2.11	27.19		142.47		1.51	92.11	1.36
6500.0	2.36	28.81		7.44		1.48	93.85	1.35
6750.0	2.57	29.66		-124.81		1.45	79.45	1.33
7000.0	2.64	29.87	-1.36	107.21	28.97	1.40	83.75	1.31
7250.0	2.54	29.63	-1.12	-16.93	13.13	1.36	83.78	1.29
7500.0	2.29	29.17	-.67	-136.97	1.39	1.31	80.58	1.27
7750.0	2.02	28.76	-.25	107.49	-5.85	1.26	81.43	1.26
8000.0	1.78	28.24	.25	-3.28	-8.31	1.22	91.88	1.23
8250.0	1.60	28.13	.37	-112.78	-9.52	1.22	90.51	1.22
8500.0	1.48	28.09	.40	137.19	-11.25	1.22	93.19	1.18
8750.0	1.43	28.11	.39	27.18	-12.97	1.22	87.65	1.14
9000.0	1.41	28.03	.46	-82.09	-13.94	1.20	88.30	1.10
9250.0	1.38	27.85	.65	170.32	-13.24	1.20	87.03	1.06
9500.0	1.36	27.75	.74	62.79	-12.47	1.18	85.20	1.07
9750.0	1.31	27.56	.94	-42.85	-9.81	1.17	86.66	1.13
10000.0	1.28	27.45	1.05	-147.28	-5.95	1.16	102.47	1.20
10250.0	1.25	27.56	.93	108.26	-2.10	1.16	83.70	1.27
10500.0	1.25	27.94	.56	4.51	2.42	1.17	80.71	1.30
10750.0	1.27	28.46	.03	-101.91	4.29	1.18	91.98	1.27
11000.0	1.28	28.75	-.25	151.62	6.12	1.19	87.45	1.23
11250.0	1.29	28.87	-.36	43.60	6.40	1.19	82.82	1.22
11500.0	1.34	28.89	-.39	-62.42	8.69	1.18	85.20	1.27
11750.0	1.41	29.13	-.62	-168.55	10.86	1.19	84.77	1.35
12000.0	1.49	29.23	-.73	82.84	10.54	1.21	82.25	1.40
12250.0	1.57	29.02	-.52	-26.10	9.90	1.21	75.42	1.43
12500.0	1.64	28.99	-.48	-134.34	9.96	1.21	89.20	1.38
12750.0	1.68	28.91	-.41	116.97	9.56	1.20	82.46	1.35
13000.0	1.69	28.81	-.31	8.92	9.81	1.21	84.38	1.31
13250.0	1.66	28.82	-.32	-101.56	7.63	1.22	94.50	1.27
13500.0	1.60	28.63	-.13	149.47	6.96	1.22	92.48	1.26
13750.0	1.50	28.57	-.06	39.05	4.83	1.22	85.03	1.29
14000.0	1.40	28.27	.22	-70.53	3.55	1.23	84.32	1.36
14250.0	1.30	28.29	.21	177.14	-.48	1.25	92.71	1.46
14500.0	1.16	28.19	.30	63.64	-5.68	1.28	92.66	1.56
14750.0	1.05	28.37	.12	-54.02	-15.04	1.33	98.79	1.63
15000.0	1.12	28.15	.34	-175.70	-28.42	1.38	81.54	1.62
15250.0	1.19	27.35		58.27		1.42	79.02	1.50
15500.0	1.20	25.13		-71.78		1.41	71.58	1.38
15750.0	1.16	21.88		164.60		1.34	62.24	1.31
16000.0	1.13	17.73		46.71		.00	53.72	1.16

LINEAR-IZATION RANGE	7000.0 TO 15000.0	7000.0 TO 15000.0

TABLE XXI

JUNE 3, 1976

7-15 GASFET AMPLIFIER

S/N 2

FREQ MHZ	VSWR IN	GAIN DB	FLAT DB	PHASE DEG	PHASE DEV	GPDEL NSEC	ISOL DB	VSWR OUT
6000.0	1.48	23.45		-89.04		.00	95.54	1.64
6250.0	1.34	26.05		134.97		1.52	80.85	1.59
6500.0	1.40	27.80		-2.17		1.50	87.15	1.56
6750.0	1.65	28.51		-135.62		1.45	86.81	1.51
7000.0	1.96	28.39	-1.16	96.54	25.32	1.39	86.44	1.46
7250.0	2.19	27.04	-.61	-25.90	11.26	1.33	82.48	1.41
7500.0	2.25	27.40	-.16	-142.95	2.58	1.28	84.04	1.36
7750.0	2.14	27.22	.00	103.65	-2.43	1.25	82.34	1.31
8000.0	1.93	27.06	.16	-7.16	-4.88	1.23	89.75	1.24
8250.0	1.71	27.23	.00	-117.45	-6.80	1.23	92.06	1.20
8500.0	1.52	27.37	-.13	130.33	-10.04	1.24	87.99	1.17
8750.0	1.42	27.41	-.17	19.05	-13.55	1.24	83.23	1.15
9000.0	1.38	27.31	-.07	-91.54	-15.77	1.22	88.46	1.15
9250.0	1.36	27.01	.21	159.62	-16.23	1.21	91.15	1.18
9500.0	1.37	26.78	.44	51.07	-16.40	1.20	89.47	1.21
9750.0	1.36	26.36	.86	-55.59	-14.69	1.18	88.19	1.24
10000.0	1.33	25.99	1.23	-160.75	-11.47	1.16	86.22	1.26
10250.0	1.29	25.81	1.41	94.89	-7.46	1.15	87.18	1.28
10500.0	1.25	25.82	1.40	-7.32	-1.29	1.15	86.76	1.27
10750.0	1.25	26.10	1.12	-111.29	3.09	1.15	85.72	1.24
11000.0	1.32	26.40	.82	145.13	7.89	1.16	85.76	1.21
11250.0	1.43	26.76	.46	39.09	10.23	1.18	79.91	1.19
11500.0	1.50	26.99	.23	-66.76	12.75	1.18	96.16	1.19
11750.0	1.51	27.35	-.12	-173.05	14.83	1.19	86.32	1.20
12000.0	1.47	27.51	-.28	78.58	14.83	1.20	81.33	1.19
12250.0	1.42	27.57	-.34	-29.57	15.05	1.21	77.86	1.19
12500.0	1.39	27.66	-.43	-138.73	14.27	1.21	87.22	1.16
12750.0	1.41	27.67	-.43	112.70	14.08	1.21	83.22	1.16
13000.0	1.46	27.70	-.47	4.04	13.79	1.22	80.55	1.17
13250.0	1.46	27.81	-.58	-106.60	11.52	1.22	87.56	1.22
13500.0	1.41	27.81	-.58	144.15	10.65	1.23	95.66	1.32
13750.0	1.35	27.99	-.75	32.00	6.89	1.24	82.80	1.45
14000.0	1.30	27.86	-.62	-79.34	3.93	1.26	85.60	1.59
14250.0	1.28	27.94	-.71	165.36	-2.98	1.28	93.35	1.72
14500.0	1.27	27.69	-.46	49.64	-10.33	1.31	105.09	1.81
14750.0	1.25	27.63	-.40	-70.79	-22.38	1.35	91.12	1.84
15000.0	1.22	27.07	.16	166.95	-36.26	1.37	80.39	1.77
15250.0	1.24	25.98		41.97		1.40	80.60	1.69
15500.0	1.24	24.32		-85.77		1.40	82.69	1.64
15750.0	1.19	21.85		149.45		1.39	67.78	1.60
16000.0	1.12	18.98		24.58		.00	58.50	1.45

LINEAR-IZATION RANGE	7000.0 TO 15000.0	7000.0 TO 15000.0

TABLE XXII

JUNE 3, 1976

7-15 GASFET AMPLIFIER

S21 IN DB

FREQ	S/N 1 GAIN	PHASE	DG12	DP12	S/N 2 GAIN	PHASE
7000.0	29.87	107.2	1.48	10.7	28.39	96.5
7250.0	29.63	-16.9	1.78	9.0	27.84	-25.9
7500.0	29.17	-137.0	1.78	6.0	27.40	-143.0
7750.0	28.76	107.5	1.53	3.8	27.22	103.7
8000.0	28.24	-3.3	1.18	3.9	27.06	-7.2
8250.0	28.13	-112.8	.89	4.7	27.23	-117.5
8500.0	28.09	137.2	.73	6.3	27.37	130.9
8750.0	28.11	27.2	.70	8.1	27.41	19.1
9000.0	28.03	-82.1	.73	9.5	27.31	-91.5
9250.0	27.85	170.3	.84	10.7	27.01	159.6
9500.0	27.75	62.8	.97	11.7	26.78	51.1
9750.0	27.56	-42.9	1.19	12.7	26.36	-55.6
10000.	27.45	-147.3	1.46	13.5	25.99	-160.7
10250.	27.56	108.3	1.75	13.4	25.81	94.9
10500.	27.94	4.5	2.11	11.8	25.82	-7.3
10750.	28.46	-101.9	2.36	9.4	26.10	-111.3
11000.	28.75	151.6	2.35	6.5	26.40	145.1
11250.	28.87	43.6	2.11	4.5	26.76	39.1
11500.	28.89	-62.4	1.90	4.3	26.99	-66.8
11750.	29.13	-168.5	1.78	4.5	27.35	-173.0
12000.	29.23	82.8	1.72	4.3	27.51	78.6
12250.	29.02	-26.1	1.45	3.5	27.57	-29.6
12500.	28.99	-134.3	1.33	4.4	27.66	-138.7
12750.	28.91	117.0	1.25	4.3	27.67	112.7
13000.	28.81	8.9	1.11	4.9	27.70	4.0
13250.	28.82	-101.6	1.01	5.0	27.81	-106.6
13500.	28.63	149.5	.82	5.3	27.81	144.1
13750.	28.57	39.1	.58	7.1	27.99	32.0
14000.	28.27	-70.5	.42	8.8	27.86	-79.3
14250.	28.29	177.1	.35	11.8	27.94	165.4
14500.	28.19	63.6	.50	14.0	27.69	49.6
14750.	28.37	-54.0	.74	16.8	27.63	-70.8
15000.	28.15	-175.7	1.08	-343 17.3	27.07	167.0

TABLE XXIII

nearly the same as seen in Figure 67. This corresponds more closely to data taken on the individual modules before assembly. Figure 67 also shows how the noise figure increases beyond the band edges.

E. Amplifier In 2X2X12 Chassis

1. Comparison of Measured Data with Electrical Specifications

Table XXIV gives a comparison of the measured data on the amplifiers in the 2X2X12 inch chassis with the electrical specifications. The amplifiers met the specifications for gain, gain variation, power output at 1 dB gain compression, spurious output, reverse isolation, and 3rd order intercept points.

The noise figure was above specification for frequencies above 12 GHz.

The phase deviation from linear was less than ±16.25 degrees from 7250 to 14,500 for both amplifiers. There were peaks at 7 and 15 GHz of approximately ±30 degrees.

The input VSWR for both amplifiers was less than 2.0:1 at 7.5 GHz and above.

The phase matching was not centered about zero degrees. There was a variation of ±7 degrees centered about an offset of +5 degrees.

TABLE XXIV

Comparison of Measured Data with Specifications

Amplifier in 2X2X12 Chassis

	Spec	S/N 1	S/N 2
Gain	25 dB min	27.4 dB min	25.4 dB min
Gain Variation	±1.5 dB max	±1.25 dB	±1.36 dB
Noise Figure	10 dB max	10.7 dB max	10.4 dB max
Power Output	+6 dBm	+10 dBm min	+9 dBm min
Phase Deviation	±10° max	±29°	±30°
Input VSWR	2.0:1 max	2.75:1	2.16:1
Output VSWR	2.0:1 max	1.79:1	2.01:1
Spurious	40 dB down	None found	None measured
Reverse Isolation	50 dB min	>70 dB	>70 dB
3rd Order Intercept Point	+20 dBm	+20.5 dBm min	+20.5 dBm min
Phase Matching	≤5°	+11.9 to -1.8, +5°±7°	
Safe Input Power			
CW RF	+30 dBm min	(+30 dBm min)	
10% Duty Peak Pulse	+50 dBm min	(+50 dBm min, 1% duty cycle 1 μs Pulse)	

2. Measured Data - Room Temperature

Tables XXV and XXVI show ANA data on the amplifiers in the 2X2X12 chassis. Table XXVII shows phase and gain match between the two amplifiers. Absolute phase matching was slightly improved over the performance shown in Table XXIII by interchanging the lengths of coaxial cable. Note that the phase match would be appreciably improved by adding a phase offset of 5° to S/N 2.

Noise figure versus frequency on the two units is shown in Figure 68. For comparison, the noise figures of the units before the addition of the limiter and cables is also shown. Saturated power (with input power of 0 dBm), 1 dB compression point, and 3rd order intercept points are shown in Figures 69 and 70.

Spurious output was measured on S/N 1 by applying an input signal on the input which gave 10 dBm of power at the output. The output was then examined on the spectrum analyzer for any additional spurious signals. The only signals found were second harmonics which are shown in Table XXVIII.

3. Data over Temperature

Gain, noise figure, and 1 dB gain compression were measured at -28°C and +65°C. Gain versus temperature on the two units is shown in Figures 71 and 72. The gain drops monotonically with increasing temperature with the change

FIGURE 68

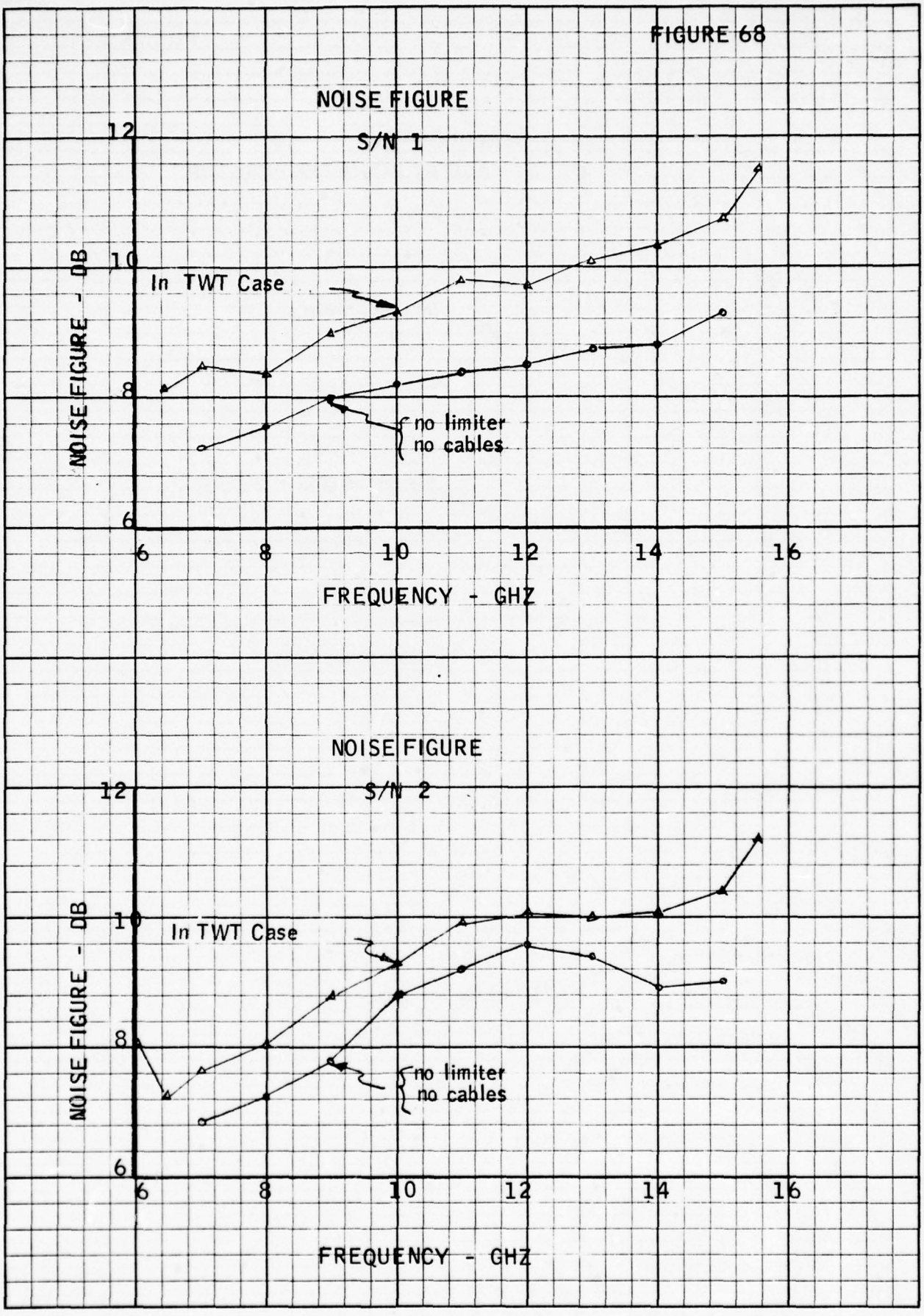

NOISE FIGURE
S/N 1
12
10
8
6
NOISE FIGURE - DB
In TWT Case
no limiter
no cables
6
8
10
12
14
16
FREQUENCY - GHZ
NOISE FIGURE
S/N 2
12
10
8
6
NOISE FIGURE - DB
In TWT Case
no limiter
no cables
6
8
10
12
14
16
FREQUENCY - GHZ

FIGURE 69

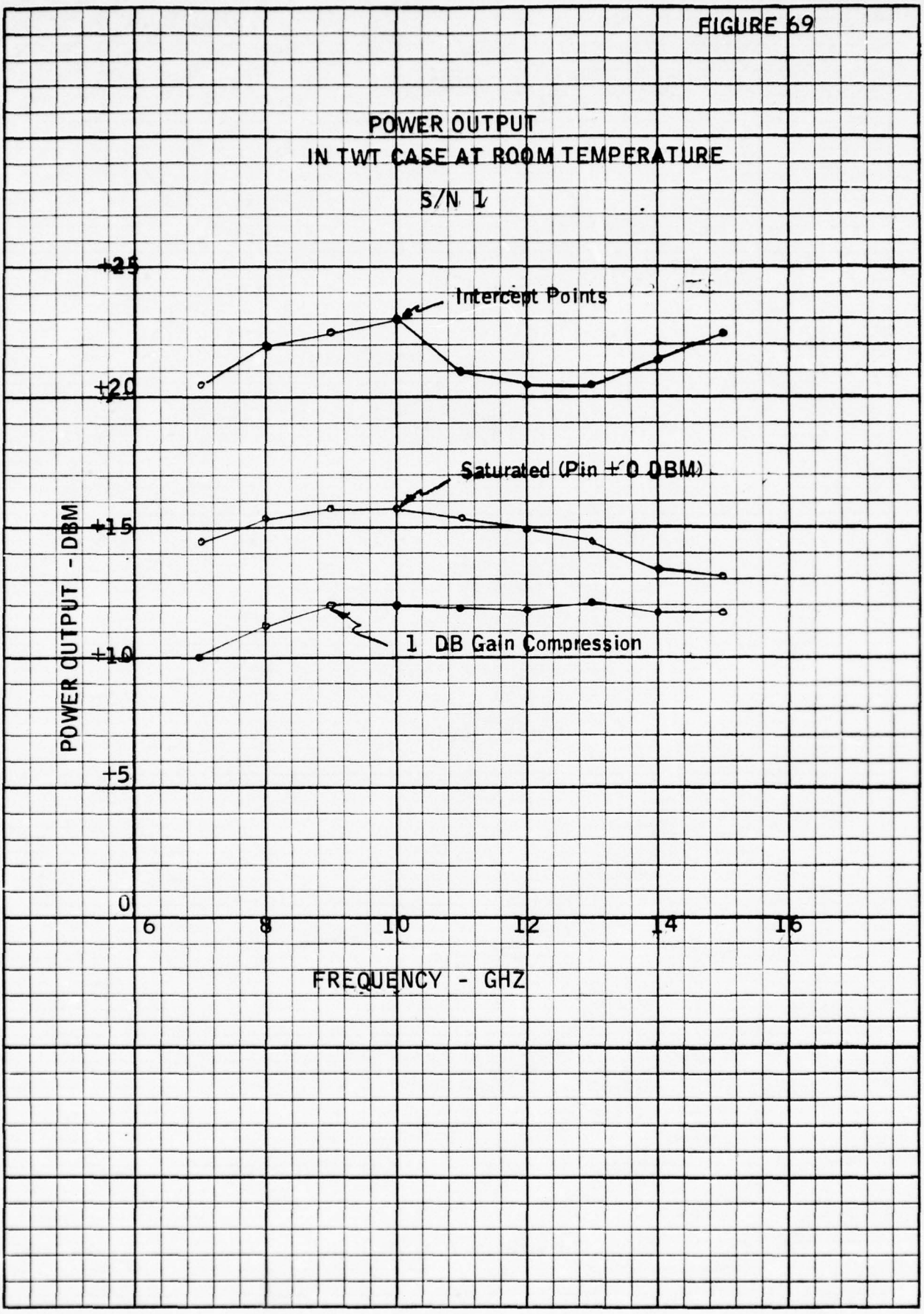
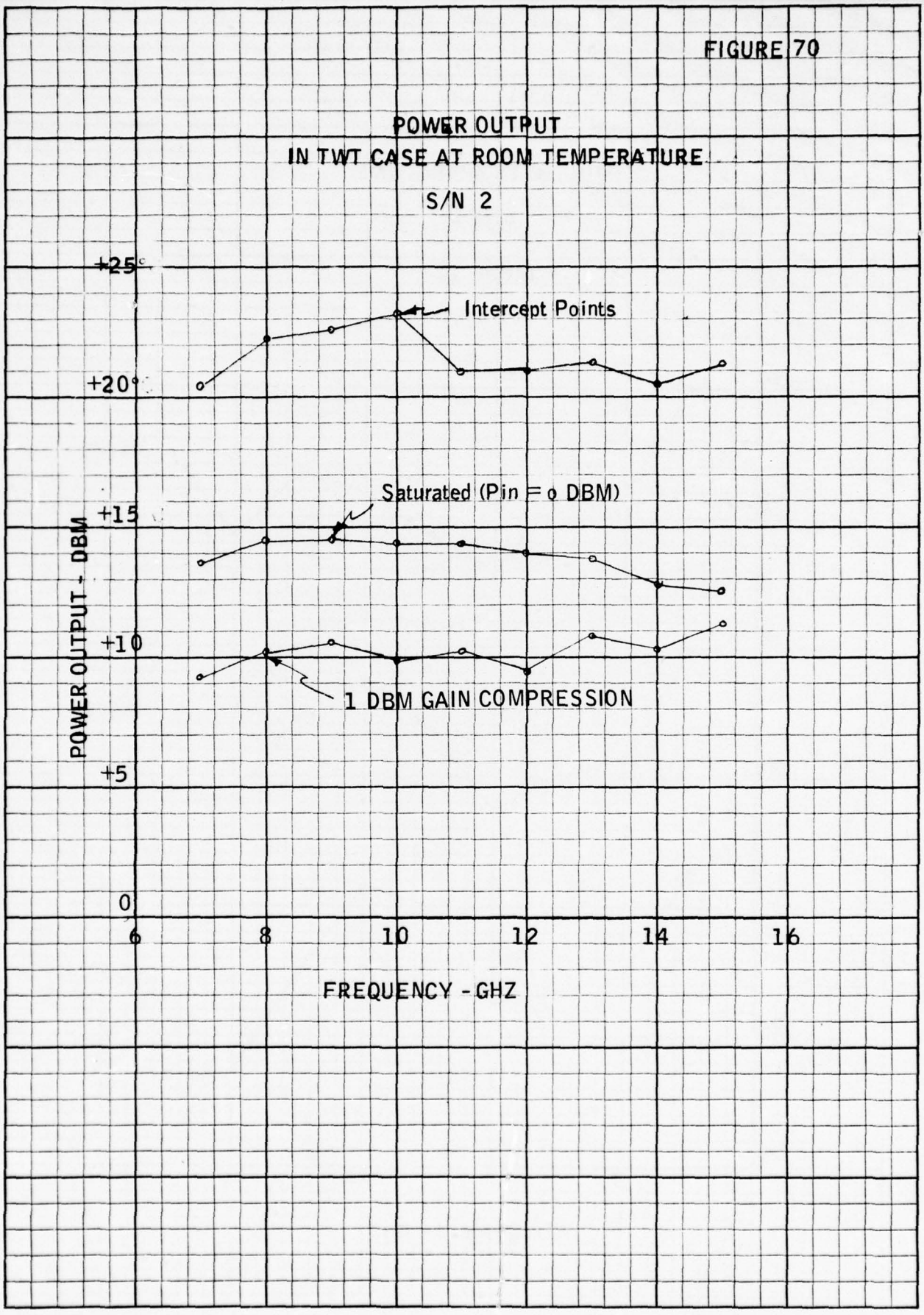

POWER OUTPUT
IN TWT CASE AT ROOM TEMPERATURE
S/N 1
Intercept Points
Saturated (Pin +0 DBM)
1 DB Gain Compression
POWER OUTPUT - DBM
+25
+20
+15
+10
+5
0
6
8
10
12
14
16
FREQUENCY - GHZ

FIGURE 70


POWER OUTPUT
IN TWT CASE AT ROOM TEMPERATURE
S/N 2
+25°
+20°
Intercept Points
Saturated (Pin = 0 DBM)
+15
+10
+5
0
POWER OUTPUT - DBM
1 DBM GAIN COMPRESSION
6
8
10
12
14
16
FREQUENCY - GHZ

GAIN vs TEMPERATURE

S/N 1

Figure 71

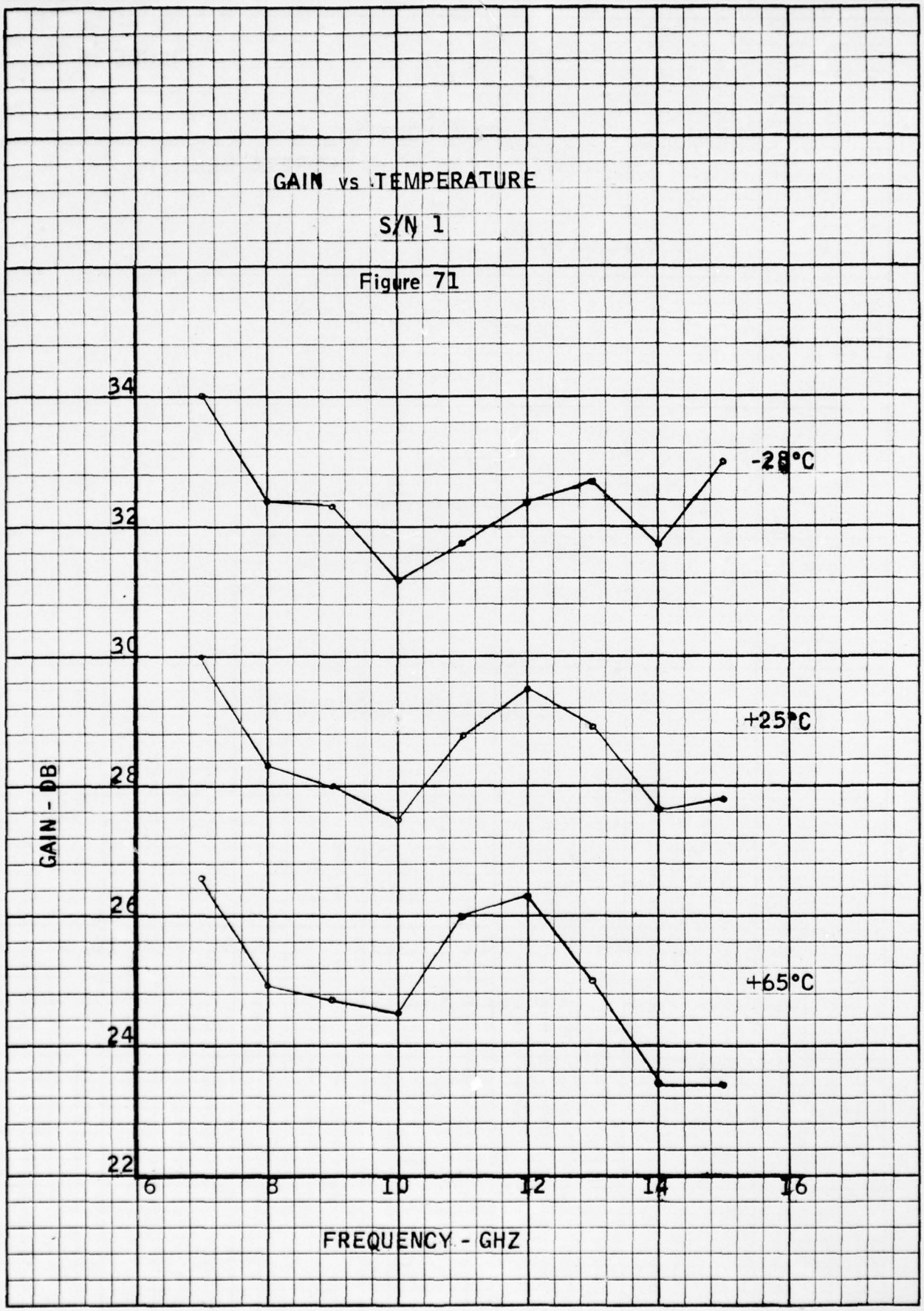
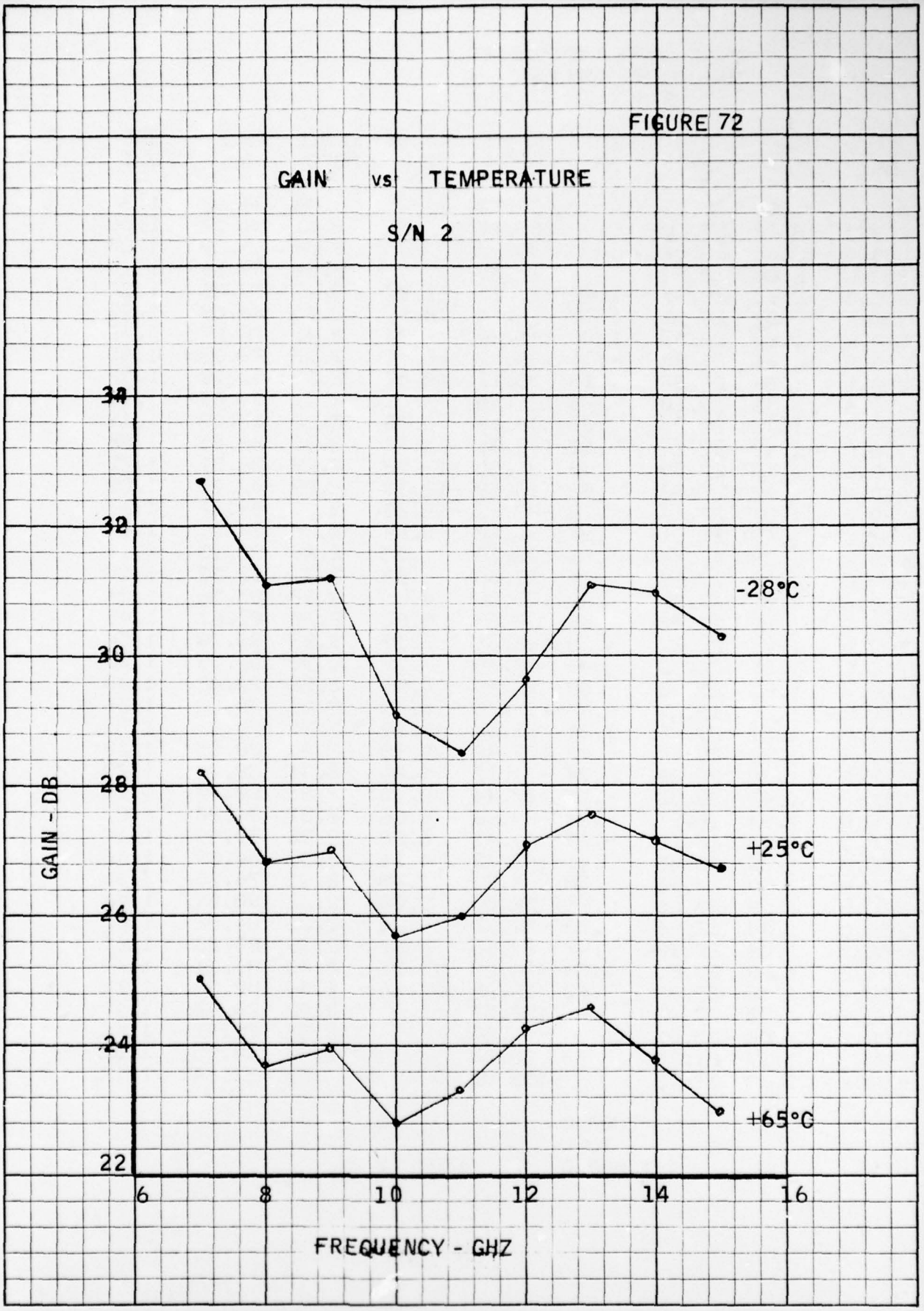


FIGURE 72

GAIN vs TEMPERATURE

S/N 2



JUNE 3, 1976

7-15 GASFET AMPLIFIER
WITH COAX CABLES
S/N 1

FREQ MHZ	VSWR IN	GAIN DB	FLAT DB	PHASE DEG	PHASE DEV	GPIEL NSEC	ISOL DB	VSWR OUT
6000.0	1.89	25.33		69.34		.00	84.38	1.26
6250.0	2.27	27.50		-167.12		2.61	81.11	1.26
6500.0	2.45	28.99		-39.95		2.58	80.29	1.27
6750.0	2.66	29.94		87.99		2.54	89.14	1.18
7000.0	2.75	29.95	-1.49	-136.84	28.77	2.49	78.36	1.36
7250.0	2.34	29.91	-1.45	-.14	12.67	2.45	84.08	1.23
7500.0	1.89	29.47	-1.00	141.36	1.36	2.41	76.87	1.42
7750.0	1.76	28.98	-.51	-73.63	-6.43	2.37	78.38	1.35
8000.0	1.66	28.27	.19	75.13	-10.47	2.32	91.10	1.27
8250.0	1.53	28.10	.35	-131.30	-9.71	2.31	94.69	1.41
8500.0	1.48	28.20	.25	19.19	-12.02	2.33	87.08	1.18
8750.0	1.48	28.16	.30	169.31	-14.71	2.31	88.65	1.26
9000.0	1.50	27.99	.46	-36.68	-13.52	2.29	88.51	1.22
9250.0	1.49	27.83	.62	116.52	-13.13	2.29	92.25	1.09
9500.0	1.51	27.74	.72	-89.63	-12.08	2.28	99.37	1.17
9750.0	1.45	27.51	.94	66.62	-8.64	2.26	84.57	1.08
10000.0	1.39	27.44	1.01	-136.75	-4.82	2.26	96.13	1.11
10250.0	1.29	27.69	.76	20.66	-.23	2.25	82.83	1.15
10500.0	1.07	27.98	.48	178.05	4.35	2.27	87.56	1.34
10750.0	1.20	28.40	.06	-27.65	5.85	2.29	87.61	1.46
11000.0	1.43	28.77	-.30	126.61	7.29	2.29	83.78	1.54
11250.0	1.55	28.88	-.42	-80.10	7.79	2.30	82.79	1.70
11500.0	1.61	29.15	-.69	73.42	8.49	2.28	94.42	1.40
11750.0	1.51	29.27	-.80	-130.78	11.48	2.29	88.62	1.54
12000.0	1.31	29.48	-1.01	21.65	11.10	2.31	90.99	1.32
12250.0	1.36	28.64	-.17	173.48	10.13	2.31	80.85	1.19
12500.0	1.38	29.20	-.74	-34.18	9.66	2.31	89.04	1.20
12750.0	1.45	29.02	-.55	117.44	8.48	2.31	80.57	1.16
13000.0	1.64	28.91	-.45	-89.66	8.56	2.31	84.80	1.27
13250.0	1.63	28.76	-.29	61.41	6.82	2.33	79.99	1.12
13500.0	1.66	28.45	.01	-148.48	4.11	2.32	84.39	1.46
13750.0	1.90	27.96	.50	3.71	3.49	2.31	76.35	1.31
14000.0	1.90	27.66	.80	156.09	3.06	2.32	80.84	1.52
14250.0	1.54	27.66	.79	-54.22	-.04	2.35	84.82	1.67
14500.0	1.26	27.99	.47	93.96	-4.67	2.39	88.23	1.61
14750.0	1.29	27.95	.50	-124.27	-15.71	2.43	87.31	1.79
15000.0	1.52	27.83	.63	16.95	-27.30	2.46	102.36	1.72
15250.0	1.53	27.07		152.57		2.52	76.45	1.43
15500.0	1.24	25.01		-76.54		2.51	73.61	1.42
15750.0	1.17	21.78		60.02		2.45	60.55	1.02
16000.0	1.28	17.33		-158.02		.00	53.84	1.12

LINEARIZATION RANGE	7000.0 TO 15000.0	7000.0 TO 15000.0

TABLE XXV

JUNE 3, 1976

7-15 GASFET AMPLIFIER
WITH COAX CABLES
S/N 2

FREQ MHZ	VSWR IN	GAIN DB	FLAT DB	PHASE DEG	PHASE DEV	GDIEL NSEC	ISOL DB	VSWR OUT
6000.0	1.40	23.34		63.08		.00	85.57	1.43
6250.0	1.29	26.06		-173.68		2.62	82.56	1.49
6500.0	1.45	27.61		-48.24		2.60	86.39	1.50
6750.0	1.65	28.49		78.61		2.55	83.51	1.36
7000.0	2.01	28.15	-1.29	-146.84	.25.02	2.48	82.46	1.55
7250.0	2.16	27.71	-.85	-8.10	10.90	2.42	81.53	1.35
7500.0	1.99	27.24	-.39	137.16	3.28	2.37	80.83	1.51
7750.0	1.88	27.12	-.26	-75.48	-2.23	2.36	84.63	1.37
8000.0	1.82	26.81	.04	72.53	-7.09	2.33	87.02	1.29
8250.0	1.69	26.89	-.04	-134.20	-6.70	2.32	91.44	1.37
8500.0	1.55	27.14	-.28	14.68	-10.69	2.35	91.41	1.10
8750.0	1.44	27.18	-.33	163.69	-14.56	2.33	95.79	1.25
9000.0	1.42	27.01	-.16	-44.01	-15.13	2.31	86.83	1.09
9250.0	1.45	26.71	.14	107.97	-16.03	2.31	83.43	1.14
9500.0	1.47	26.54	.31	-99.04	-15.92	2.29	88.56	1.10
9750.0	1.39	26.13	.72	55.67	-14.07	2.28	91.97	1.13
10000.0	1.36	25.70	1.15	-148.69	-11.31	2.26	88.39	1.20
10250.0	1.42	25.54	1.30	9.05	-6.45	2.24	89.03	1.16
10500.0	1.27	25.42	1.42	167.95	-.42	2.25	86.50	1.33
10750.0	1.10	25.66	1.19	-35.52	3.23	2.26	85.87	1.35
11000.0	1.32	26.01	.84	121.76	7.63	2.26	86.79	1.35
11250.0	1.40	26.29	.56	-82.99	10.01	2.28	83.83	1.45
11500.0	1.56	26.68	.17	71.77	11.89	2.27	106.38	1.26
11750.0	1.71	26.86	-.01	-131.93	15.33	2.28	82.59	1.31
12000.0	1.57	27.07	-.22	21.82	16.20	2.30	85.83	1.28
12250.0	1.41	26.64	.21	174.49	15.99	2.31	82.21	1.05
12500.0	1.39	27.31	-.46	-33.20	15.43	2.31	87.73	1.18
12750.0	1.32	27.38	-.52	119.25	15.00	2.31	77.29	1.14
13000.0	1.23	27.56	-.70	-88.59	14.28	2.32	91.28	1.22
13250.0	1.24	27.58	-.72	61.69	11.69	2.33	84.84	1.16
13500.0	1.29	27.42	-.56	-148.67	8.45	2.33	83.87	1.58
13750.0	1.54	27.34	-.48	1.79	6.04	2.34	81.88	1.36
14000.0	1.59	27.14	-.28	150.82	2.20	2.35	89.89	1.72
14250.0	1.44	27.13	-.27	-62.00	-3.48	2.38	102.95	1.80
14500.0	1.47	27.23	-.37	83.13	-11.23	2.41	91.91	1.76
14750.0	1.49	26.85	.00	-135.30	-22.54	2.43	86.36	2.01
15000.0	1.33	26.69	.16	5.35	-34.75	2.47	91.37	1.78
15250.0	1.12	25.66		140.90		2.51	78.68	1.69
15500.0	1.13	23.95		-85.86		2.51	89.40	1.63
15750.0	1.16	21.57		49.72		2.50	71.02	1.27
16000.0	1.11	18.56		-174.97		.00	59.39	1.33

LINEAR-IZATION RANGE	7000.0 TO 15000.0	7000.0 TO 15000.0

TABLE XXVI

JUNE 3, 1976

7-15 GASFET AMPLIFIER
WITH COAX CABLES

S21 IN DB

FREQ	S/N 1 GAIN	PHASE	DG12	DP12	S/N 2 GAIN	PHASE
7000.0	29.95	-136.8	1.81	10.0	28.15	-146.8
7250.0	29.91	-.1	2.20	8.0	27.71	-8.1
7500.0	29.47	141.4	2.22	4.2	27.24	137.2
7750.0	28.98	-73.6	1.86	1.9	27.12	-75.5
8000.0	28.27	75.1	1.47	2.6	26.81	72.5
8250.0	28.10	-131.3	1.21	2.9	26.89	-134.2
8500.0	28.20	19.2	1.06	4.5	27.14	14.7
8750.0	28.16	169.3	.97	5.6	27.18	163.7
9000.0	27.99	-36.7	.98	7.3	27.01	-44.0
9250.0	27.83	116.5	1.12	8.5	26.71	108.0
9500.0	27.74	-89.6	1.20	9.4	26.54	-99.0
9750.0	27.51	66.6	1.38	11.0	26.13	55.7
10000.	27.44	-136.7	1.74	11.9	25.70	-148.7
10250.	27.69	20.7	2.15	11.6	25.54	9.0
10500.	27.98	178.1	2.56	10.1	25.42	167.9
10750.	28.40	-27.6	2.74	7.9	25.66	-35.5
11000.	28.77	126.6	2.76	4.8	26.01	121.8
11250.	28.88	-80.1	2.60	2.9	26.29	-83.0
11500.	29.15	73.4	2.47	1.6	26.68	71.8
11750.	29.27	-130.8	2.40	1.1	26.86	-131.9
12000.	29.48	21.6	2.40	-.2	27.07	21.8
12250.	28.64	173.5	2.01	-1.0	26.64	174.5
12500.	29.20	-34.2	1.89	-1.0	27.31	-33.2
12750.	29.02	117.4	1.64	-1.8	27.38	119.2
13000.	28.91	-89.7	1.35	-1.1	27.56	-88.6
13250.	28.76	61.4	1.18	-.3	27.58	61.7
13500.	28.45	-148.5	1.03	.2	27.42	-148.7
13750.	27.96	3.7	.62	1.9	27.34	1.8
14000.	27.66	156.1	.52	5.3	27.14	150.8
14250.	27.66	-54.2	.54	7.8	27.13	-62.0
14500.	27.99	94.0	.76	10.8	27.23	83.1
14750.	27.95	-124.3	1.10	11.0	26.85	-135.3
15000.	27.83	16.9	1.14	11.6	26.69	5.4

TABLE XXVII

TABLE XXVIII

Spurious Signals, S/N 1

Fundamental Output to Spectrum Analyzer = +10 dBm

Fundamental Frequency	2nd Harmonic Level
5.5 GHz	18 dB down
6.0 GHz	13 dB down
6.5 GHz	14 dB down
7.0 GHz	18 dB down
7.5 GHz	22 dB down
8.0 GHz	28 dB down
8.5 GHz	30 dB down
9.0 GHz	>40 dB down

No spurious signals detected.

being about 0.015 dB/°C/stage. This agrees with data taken on lower frequency FET amplifiers.

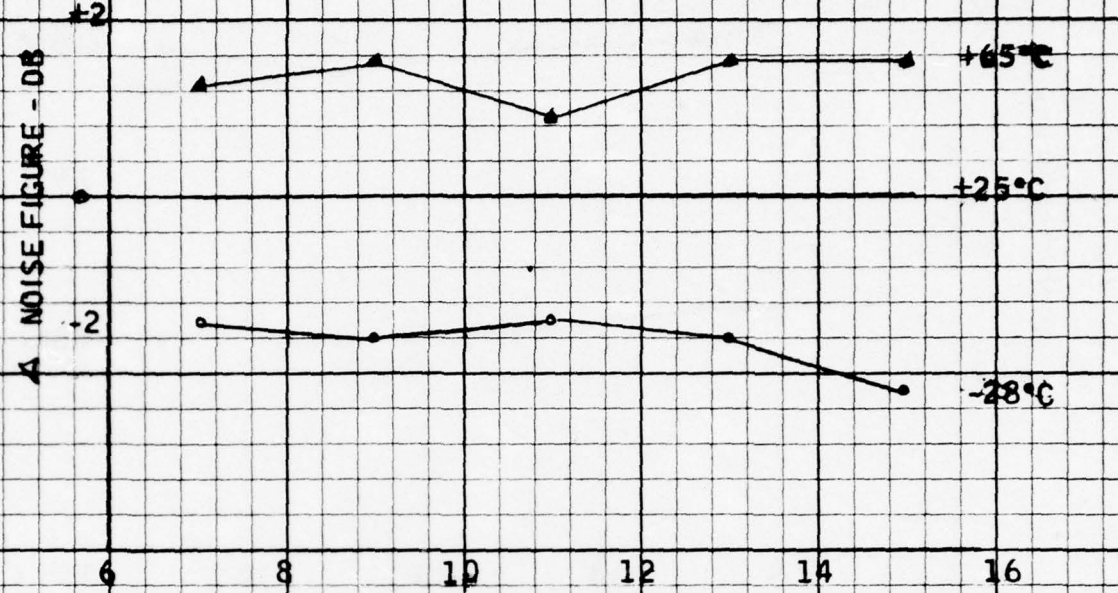
The change in both noise figure and 1 dB gain compression over temperature is shown in Figures 73 and 74.

Noise figure increases with temperature with a coefficient of 0.035 - 0.05 dB/°C. 1 dB compression changed only slightly with temperature.

FIGURE 73

CHANGE IN NOISE FIGURE WITH TEMPERATURE

S/N 1



CHANGE IN POWER OUTPUT AT 1 DB
GAIN COMPRESSION WITH TEMPERATURE

S/N 1

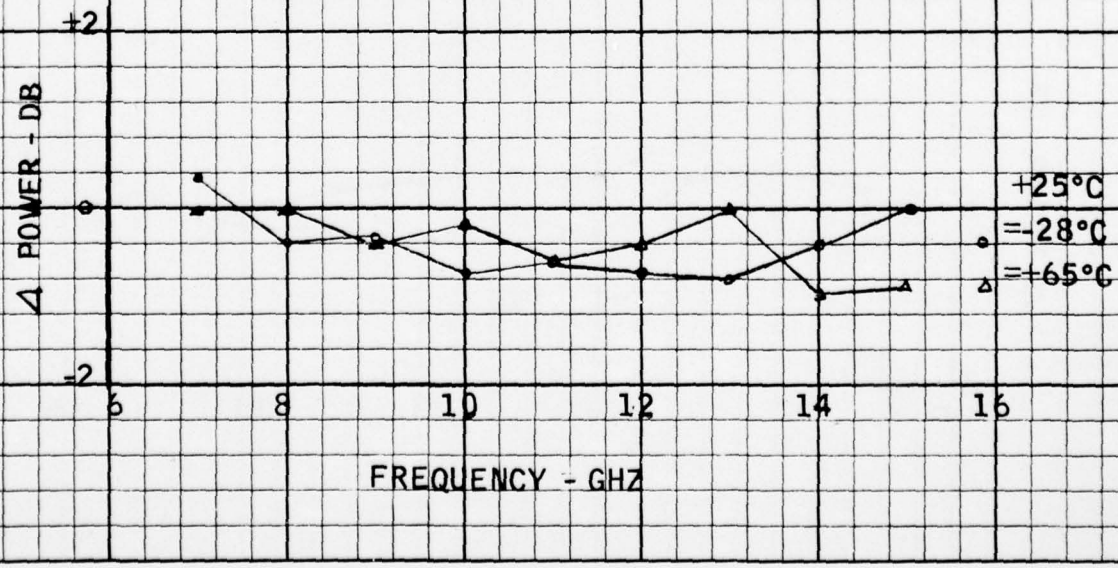
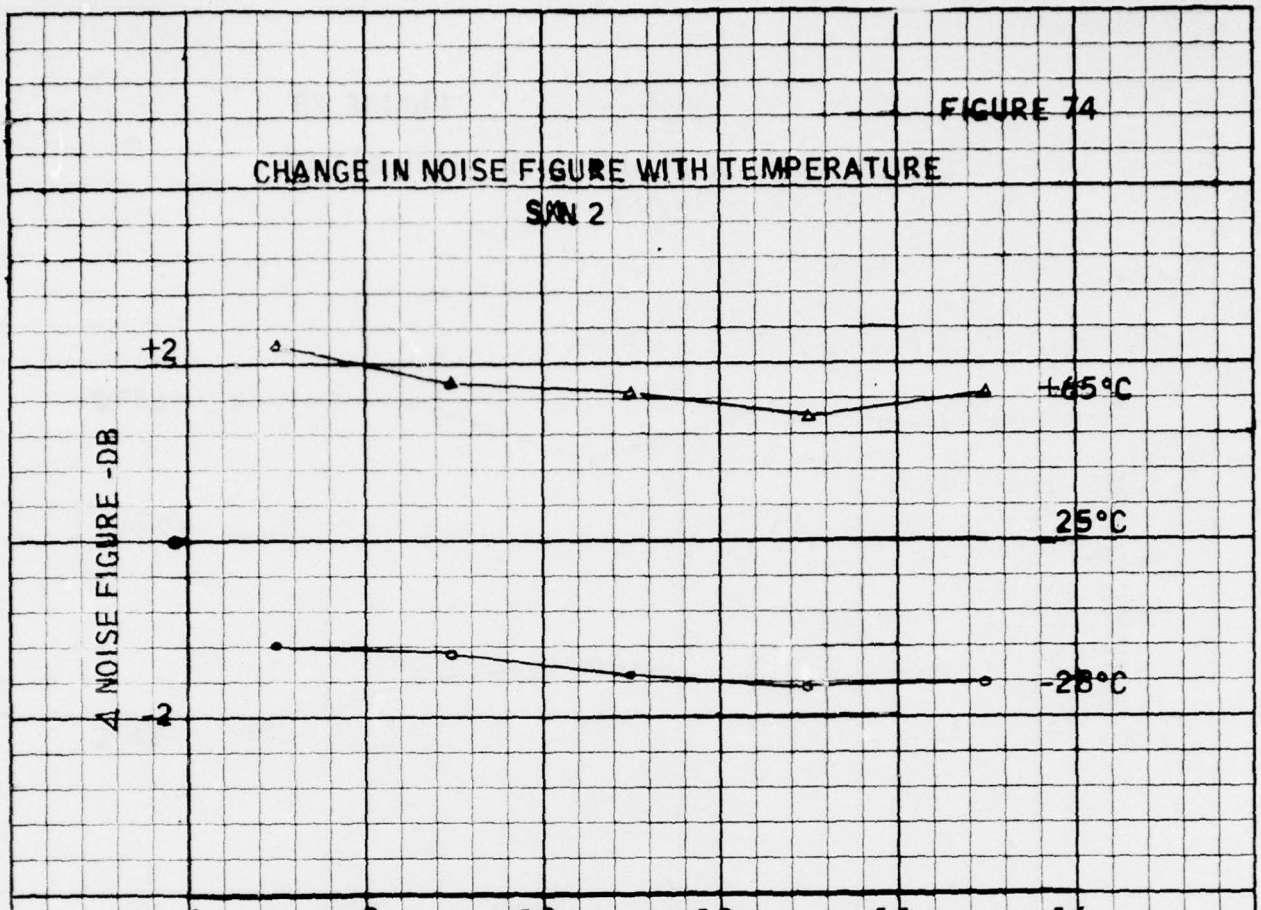


FIGURE 74

CHANGE IN NOISE FIGURE WITH TEMPERATURE
S/N 2



CHANGE IN POWER OUTPUT AT 1DB GAIN
COMPRESSION WITH TEMPERATURE
S/N 2

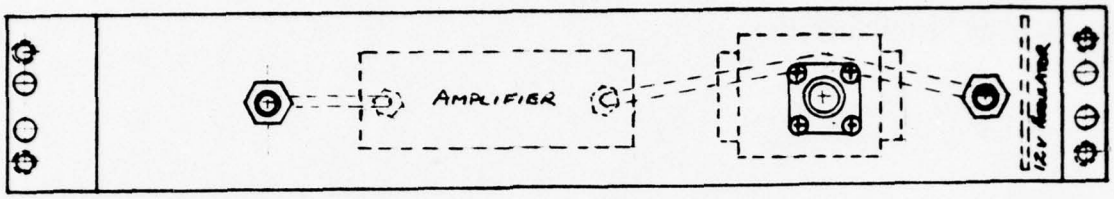
4. Drawings

Figure 75 is an assembly drawing of the 2X2X12 inch chassis. The location of the amplifier, power transformer, and 12 volt regulator can be seen.

Figure 76 is an Installation Drawing.

ASSEMBLY DRAWING

2 x 2 x 12 CHASIS



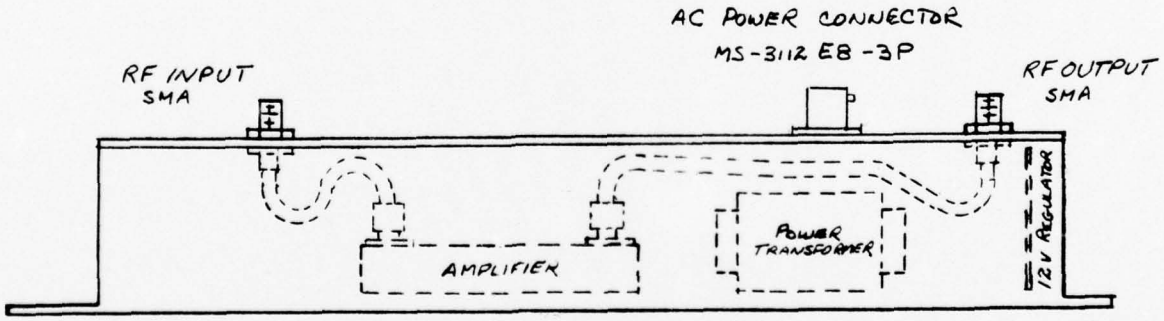


Figure 75

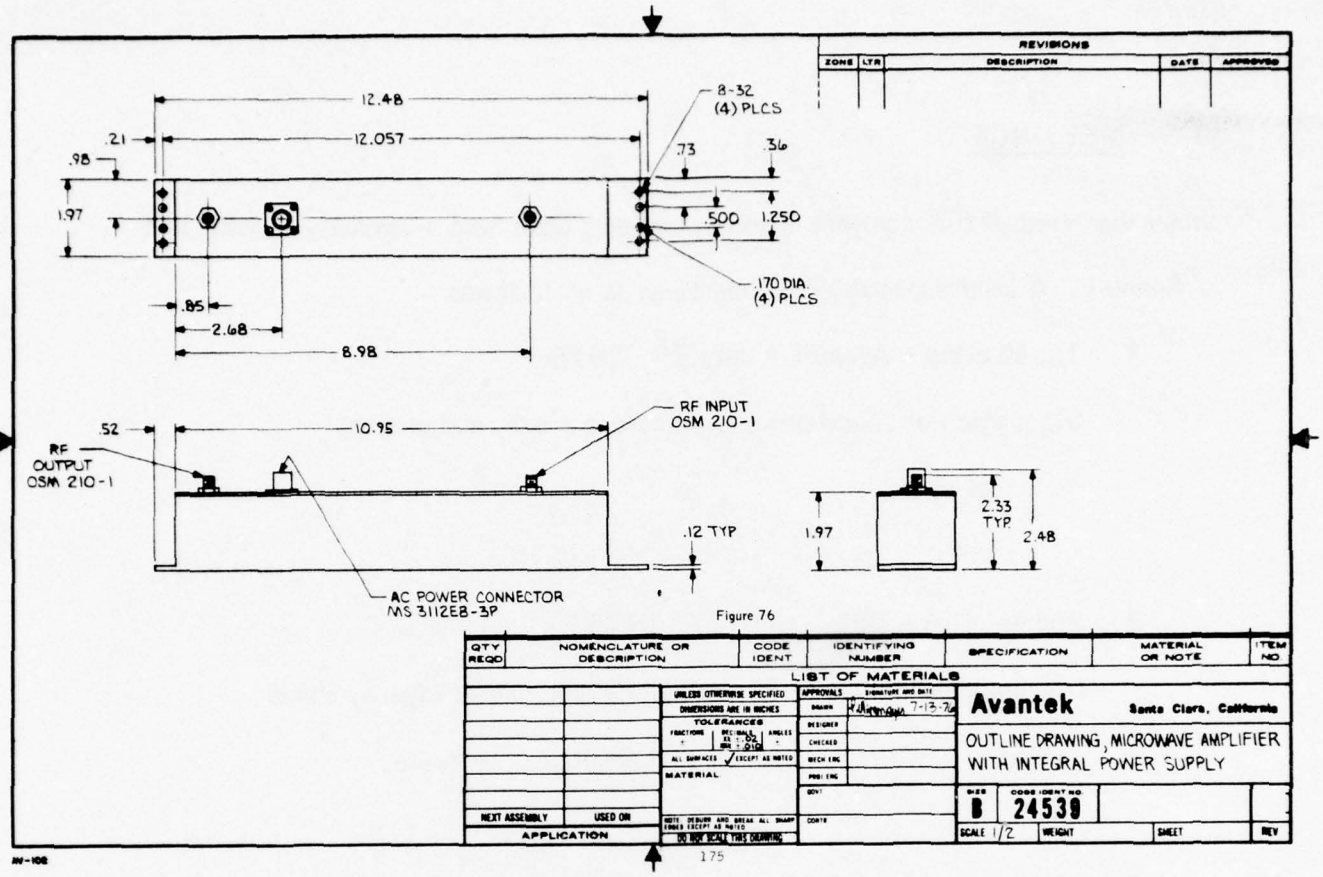

REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
12.48
12.057
.21
.98
1.97
8-32
(4) PLCS
.73
.36
.500
1.250
.170 DIA
(4) PLCS
.85
2.68
8.98
.52
10.95
RF INPUT
OSM 210-1
RF
OUTPUT
OSM 210-1
.12 TYP
AC POWER CONNECTOR
MS 3112EB-3P
1.97
2.33
TYP
2.48
QTY REQD
NOMENCLATURE OR DESCRIPTION
CODE IDENT
IDENTIFYING NUMBER
SPECIFICATION
MATERIAL OR NOTE
ITEM NO
LIST OF MATERIALS
NEXT ASSEMBLY
USED ON
APPLICATION
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
MATERIAL
APPROVALS
DRAWN
DESIGNER
CHECKED
MECH ENG
PROJ ENG
QUAL
CONTR
DO NOT SCALE THIS DRAWING
Avantek
Santa Clara, California
OUTLINE DRAWING, MICROWAVE AMPLIFIER WITH INTEGRAL POWER SUPPLY
SIZE
B
CODE IDENT NO
24539
SCALE 1/2
WEIGHT
SHEET
REV
AV-108

Figure 76

VI. MEETINGS

Under the terms of this contract quarterly reviews were held alternately at NRL and at Avantek. A brief summary of the meetings is as follows:

1. 1st Meeting - Avantek - July 29, 1975

   Discussion of specification, milestone chart, and general technical plan.

2. 2nd Meeting - NRL - Oct. 21, 1975

   Discussion included 1/2 μm FET design, buffer layers, ohmic contacts, module performance and amplifier enclosure.

3. 3rd Meeting - Avantek - Jan 20, 1976

   Discussion covered new 1/2 μm mask, buffer layers, contacts, metalization, substrate materials, coupler performance, and device characterization.

4. 4th Meeting - NRL - April 28, 1976

   Discussion of FET performance, buffer performance, implantation of active layers, new 1/2 μm geometry, new gate metal, quartz substrates, 7-15 GHz module, and limiter.

VIII. REFERENCES

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4. Mattes, B.L.et. al., Journal of Vacuum Science Technology, Volume 12, No. 4, July - Aug., 1975

5. Kurokowa, K. "Design Theory of Balanced Transitor Amplifiers", B.S.T.J., October 1965

6. Lange, J., "Interdigitated Stripling Quadration Hybrid", IEEE Trans. on MTT, Volume MTT17, Page 1150-1151, Dec. 1969

7. Fano, R.M., "Theoretical Limitations on the Broadband Matching of Arbitrary Impedances", Journal of the Franklin Inst.; Jan & Feb 1950

IX. KEY PERSONNEL

The following key personnel were assigned to the various areas of effort in this contract:

Administration

Mr. Richard Hejmanowski, R & D Manager: Contract Administrator

Process Development

Dr. Daniel Chen, Project Manager

Mr. William Hooper, Special Process Development

Dr. Pat Leung, FET Development

Material Development

Dr. Cheol Kim, Project Manager

Device Test & Characterization

Mr. Harry Cooke, Project Manager

Mr. John Elliot, Special Test & Fixturing

Amplifier Development

Mr. Gary Policky, Project Manager

Mr. Stuart Hennies, Amplifier Design